SV4D Direct Attach MIPI Test Module

Reference Design Guide

VERSION 1.2

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INTRODUCTION

Overview

The SV4D is a versatile, high-performance, ultra-compact test module enabling **at-speed** production testing for MIPI® Alliance interfaces. Capable of operating independently or within any ATE load board, the SV4D is ideal for deployment at wafer sort as well as final test or system-level test. With up to 4 MIPI transmit or receive ports each containing multiple data lanes, this module enables **multi-site** testing and results in significant cost-of-test savings for SOC, MCU, ASSP, image sensor, display driver IC, and ISP manufacturers.

This document describes a reference carrier test board design and other peripheral circuits that can be served as a guide to building your own load board. The test board and support logic design described here are application-specific, and they vary according to the application's requirements and operation environment.

PORTS AND CONNECTORS

Figure 1 shows a photograph of the top and bottom sides of the SV4D with each of its ports and connectors. The physical area of the SV4D is 3" by 3" (76 mm by 76 mm). The SV4D is mounted on the load board using a single mezzanine connector (J43). High-speed signals are transmitted over miniature board-to-cable assemblies.

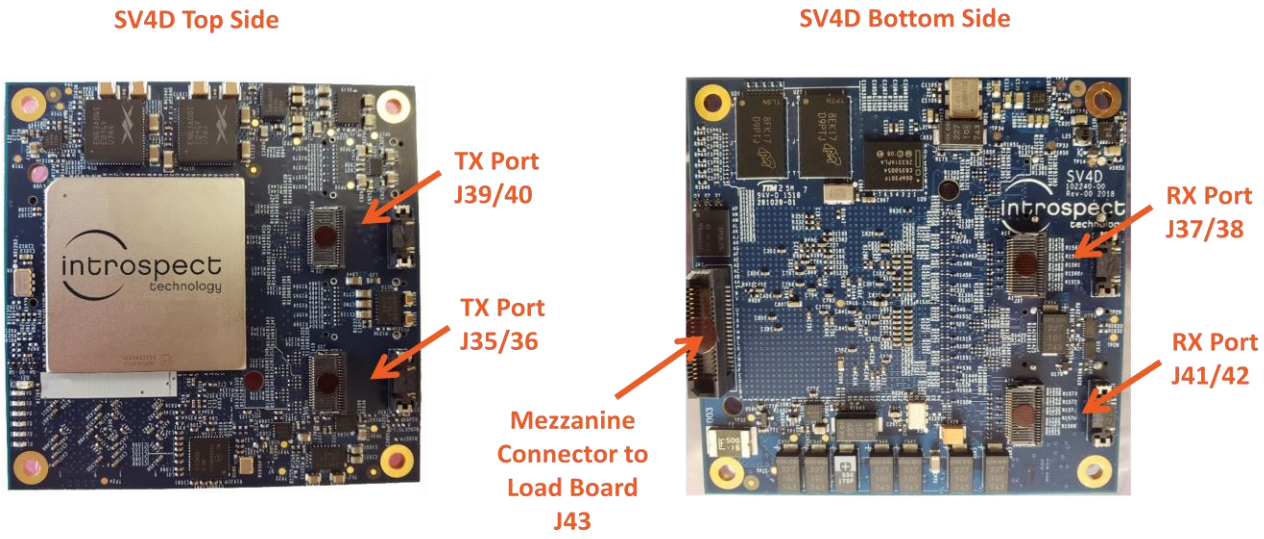


Figure 1 SV4D connectors on the top and bottom of the board

In this section, we describe the various port types and how they map into the various connectors. For reference, a legend of available port types and corresponding connector locations is included in Figure 2: J43 is the main mezzanine connector that mounts to the carrier board or load board, and J35 to J42 are board-to-cable connectors that allow for placement of the signals under test at locations that are convenient relative to DUT placement.

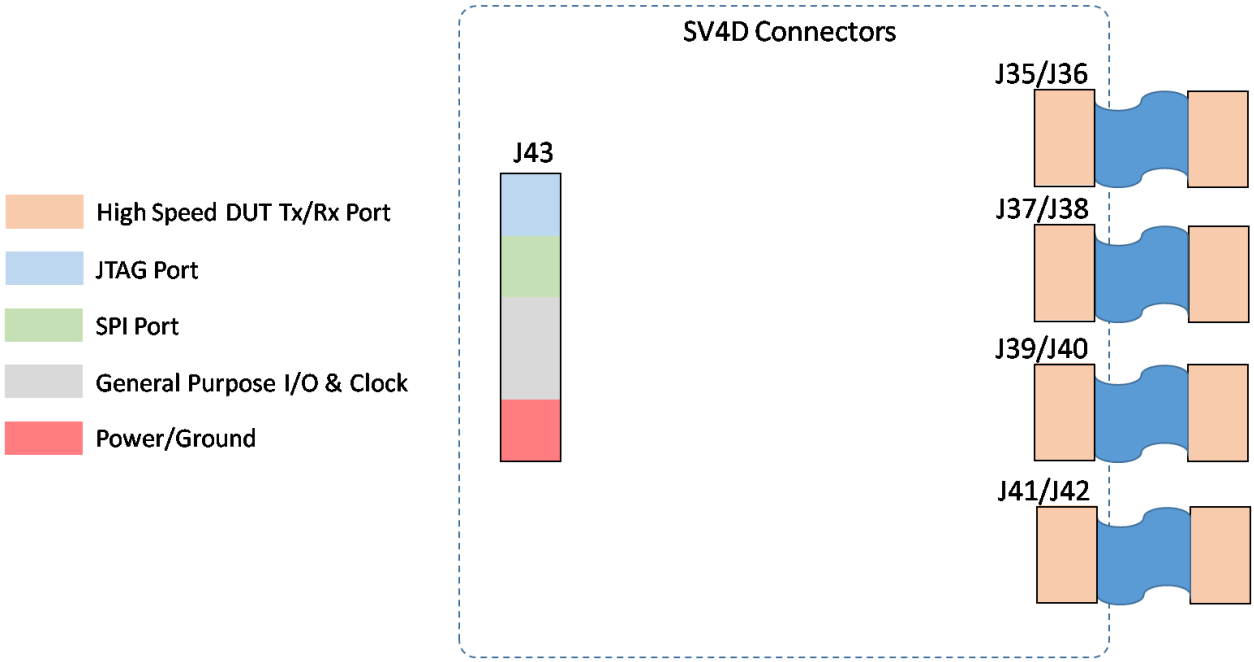


Figure 2 SV4D connector map describing the different signal and control port types

JTAG Port

The JTAG port is used for firmware update and debug. Its signals are routed on the J43 connector as per the following table:

Table 1 SV4D JTAG connectors pin-out

Connector	Pin	Net
J43	2	JTAG Port: TMS
J43	4	JTAG Port: TCK
J43	6	JTAG Port: TDO
J43	8	JTAG Port: TDI

SPI Port

The SV4D is controlled by a single SPI port facilitating transmittal of commands to the real-time operating system in the module. Table 2 shows the pin assignment of the SPI port. The SPI port acts as a slave, and it is enabled with the SSN line. Please refer to the *SV4D Command Interface Design Document* regarding the details of the SPI command interface.

Table 2 SV4D SPI port connector pin-out

Connector	Pin	Net
J43	10	SPI Port: SSN
J43	12	SPI Port: SCLK
J43	14	SPI Port: MISO
J43	16	SPI Port: MOSI

General Purpose I/O & Clock Port

Connector J43 contains a set of general purpose I/O signals that can be used for implementing custom vector programming or specialized functions. The I/O level on this port is 1.8V LVCMOS, and the detailed pinout is included in Table 3. The SV4D also allows for synchronization with an external input reference clock. 1.8 to 3.3 V LVDS is the default interface, but the SV4D can also be configured to receive CML, LVPECL, or single ended LVCMOS signals.

Table 3 SV4D general purpose i/o and clock connector pin-out

Connector	Pin	Function	Net
J43	18	Input	RESET_N
J43	20	Output	READY
J43	22	Output	FLAG_0
J43	21	Output	FLAG_1
J43	24	Input	TRIG_0
J43	23	Input	TRIG_1
J43	36	Input/Output	GPIO_0
J43	34	Input/Output	GPIO_1
J43	32	Input/Output	GPIO_2
J43	30	Input/Output	GPIO_3
J43	28	Input/Output	GPIO_4
J43	27	Input/Output	GPIO_5
J43	26	Input/Output	GPIO_6
J43	25	Input/Output	GPIO_7 / SEQUENCE_ON
J43	38	Input	CLKIN_P
J43	40	Input	CLKIN_N

Power/Ground Pins

Connector J43 also houses a single power rail for the SV4D module. The pinout for this power rail and the corresponding ground connection is listed in Table 4. All rails within the SV4D are generated internally, so there are no particular requirements on the 5V DC input.

Table 4 Power and ground pins

Connector	Pin	Net
J43	1	GND
J43	3	GND
J43	5	GND
J43	7	GND
J43	9	GND
J43	11	GND
J43	13	GND
J43	37	GND
J43	39	GND
J43	15	5V
J43	17	5V
J43	19	5V
J43	29	5V
J43	31	5V
J43	33	5V
J43	35	5V

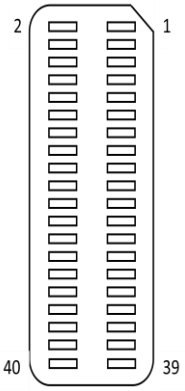
Recapitulation of the J43 Connector

For convenience, Table 5 provides a complete listing of the signals on J43, with the pinout as viewed from the top. That is, Pin 1 is located at the top right of the connector when viewed from the **top side** (component side) of the carrier board hosting the SV4D. Additional information on the connector footprints can be found on the Samtec website at the links below:

J43: Samtec Part Number ERF8-020-07.0-S-DV-K-TR
https://www.samtec.com/products/erf8-020-07.0-s-dv-k-tr

Mating connector to J43: ERM8-020-05.0-S-DV-K-TR
https://www.samtec.com/products/erm8-020-05.0-s-dv-k-tr

Table 5 Complete listing of J43 along with pin orientation

Footprint	Pin	Signal Name	Pin	Signal Name
	1	GND	21	FLAG_1
	2	JTAG TMS	22	FLAG_0
	3	GND	23	TRIG_1
	4	JTAG TCK	24	TRIG_0
	5	GND	25	SEQUENCE_ON
	6	JTAG TDO	26	GPIO_6
	7	GND	27	GPIO_5
	8	JTAG TDI	28	GPIO_4
	9	GND	29	VIN (5V)
	10	SPI SSN	30	GPIO_3
	11	GND	31	VIN (5V)
	12	SPI SCLK	32	GPIO_2
	13	GND	33	VIN (5V)
	14	SPI MISO	34	GPIO_1
	15	VIN (5V)	35	VIN (5V)
	16	SPI MOSI	36	GPIO_0
	17	VIN (5V)	37	GND
	18	RESET_N	38	CLKIN_P
	19	VIN (5V)	39	GND
	20	READY	40	CLKIN_N

High-Speed DUT Tx/Rx Ports

This section of the SV4D consists of multiple MIPI ports, each possessing 10 wires. The ports are connected to the load board using a micro flyover system from Samtec. This system consists of a two-piece connector configuration that is placed on the load board. Additional information on the connector footprints can be found on the Samtec website at the links below:

J35, J37, J39, J41: Samtec Part number UEC5-019-1-H-D-RA-1-A,
https://www.samtec.com/products/ucc8-010-1-h-s-1-a

J36, J38, J40, J42: Samtec Part Number UCC8-010-1-H-S-1-A
https://www.samtec.com/products/uec5-019-1-h-d-ra-1-a

Mating Firefly Cable Assemblies:
https://www.samtec.com/products/ecue

- Note: please use the cables provided by Introspect or ensure 1:1 pin mapping in cable assemblies to match SV4D to load board pinouts

Table 6 Signal mapping for SV4D TX Port A and B, J35/J36

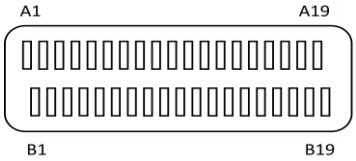
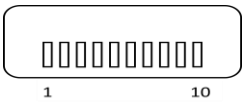
Footprint	TX PORT A		TX PORT B	
	Pin Number	**DPHY TX Signal**	**Pin Number**	**DPHY TX Signal**
J35 Part Number: Samtec UEC5-019-1-X-D-RA-1-A 	J35, A2	Data 0, P	J35, B2	Data 0, P
	J35, A3	Data 0, N	J35, B3	Data 0, N
	J35, A5	Data 1, P	J35, B5	Data 1, P
	J35, A6	Data 1, N	J35, B6	Data 1, N
	J35, A8	Data 2, P	J35, B8	Data 2, P
	J35, A9	Data 2, N	J35, B9	Data 2, N
	J35, A11	Data 3, P	J35, B11	Data 3, P
	J35, A12	Data 3, N	J35, B12	Data 3, N
	J35, A14	CLK, P	J35, B14	CLK, P
	J35, A15	CLK, N	J35, B15	CLK, N
J36 Part Number: Samtec UCC8-010-1-H-D-S-1-A 	J36	No Connections	J36	No Connections

Table 7 Signal mapping for SV4D TX Port C and D, J39/J40

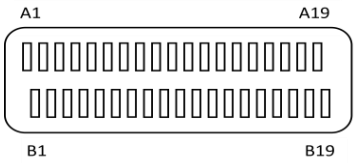
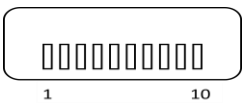
Footprint	TX PORT C		TX PORT D	
	Pin Number	**DPHY TX Signal**	**Pin Number**	**DPHY TX Signal**
J39 Part Number: Samtec UEC5-019-1-X-D-RA-1-A 	J39, A2	Data 0, P	J39, B2	Data 0, P
	J39, A3	Data 0, N	J39, B3	Data 0, N
	J39, A5	Data 1, P	J39, B5	Data 1, P
	J39, A6	Data 1, N	J39, B6	Data 1, N
	J39, A8	Data 2, P	J39, B8	Data 2, P
	J39, A9	Data 2, N	J39, B9	Data 2, N
	J39, A11	Data 3, P	J39, B11	Data 3, P
	J39, A12	Data 3, N	J39, B12	Data 3, N
	J39, A14	CLK, P	J39, B14	CLK, P
	J39, A15	CLK, N	J39, B15	CLK, N
J40 Part Number: Samtec UCC8-010-1-H-D-S-1-A 	J40	No Connections	J40	No Connections

Table 8 Signal mapping for SV4D RX Port A, J37/J38

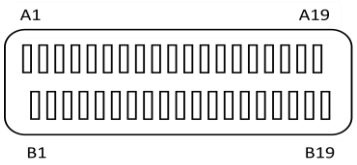
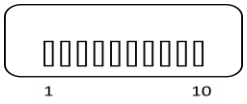
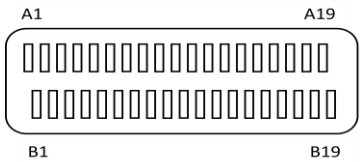
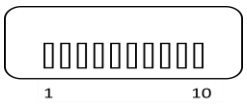
Footprint	Pin Number	RX PORT A	
		CPHY RX Signal	DPHY RX Signal
J37 Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J37, A2	Trio 0, A	Data 0, P
	J37, A5	Trio 0, B	Data 0, N
	J37, A8	Trio 0, C	Data 1, P
	J37, A11	Trio 1, A	Data 1, N
	J37, A14	Trio 1, B	Data 2, P
	J37, B2	Trio 1, C	Data 2, N
	J37, B5	Trio 2, A	Data 3, P
	J37, B8	Trio 2, B	Data 3, N
	J37, B11	Trio 2, C	CLK, P
	J37, B14	No Connection	CLK, N
J38 Part Number: Samtec UCC8-010-1-H-D-S-1-A  	J38	No Connections	No Connections

Table 9 Signal mapping for SV4D RX Port B, J41/J42

Footprint	Pin Number	RX PORT B	
		CPHY RX Signal	DPHY RX Signal
J41 Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J41, A2	Trio 0, A	Data 0, P
	J41, A5	Trio 0, B	Data 0, N
	J41, A8	Trio 0, C	Data 1, P
	J41, A11	Trio 1, A	Data 1, N
	J41, A14	Trio 1, B	Data 2, P
	J41, B2	Trio 1, C	Data 2, N
	J41, B5	Trio 2, A	Data 3, P
	J41, B8	Trio 2, B	Data 3, N
	J41, B11	Trio 2, C	CLK, P
	J41, B14	No Connection	CLK, N
J42 Part Number: Samtec UCC8-010-1-H-D-S-1-A  	J42	No Connections	No Connections

CONNECTION DIAGRAMS

JTAG Port Recommended Connections

The JTAG port is used for programming the firmware in the SV4D module. Thus, it is possible to leave all four pins of this port completely unconnected (N/C). However, the addition of a small header allows for updating firmware on the SV4D directly on the load board without having to remove it and place it on an Introspect Technology carrier board. The recommended connection diagram for this header is shown in Figure 3. The connector shown is the LX60-12S connector from Hirose, and it is illustrated in Figure 4.

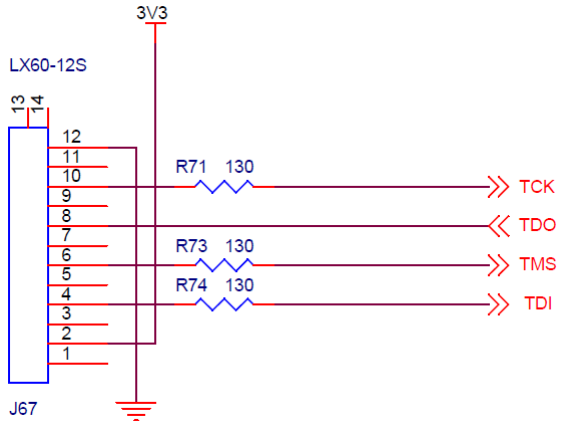


Figure 3 JTAG header connections

Figure 4 Illustration of Hirose LX60-12S connector for attaching a JTAG firmware update cable

SPI Port Recommended Connections

The simplest implementation of the SPI ports is to connect them directly to the ATE pin electronics as shown in Figure 5. There are important comments about this diagram:

- If multiple modules are used on a single load board, each SPI port uses its own SSN line, so they are both connected in a point-to-point configuration with the ATE
- Related to the above comment, since each SPI slave of the SV4D is assumed to be connected directly to a corresponding SPI master on the ATE, each MISO line is not implemented as open-drain outputs, but rather as a direct LVCMOS driver. This eliminates the need for implementing a pull-up resistor on this line

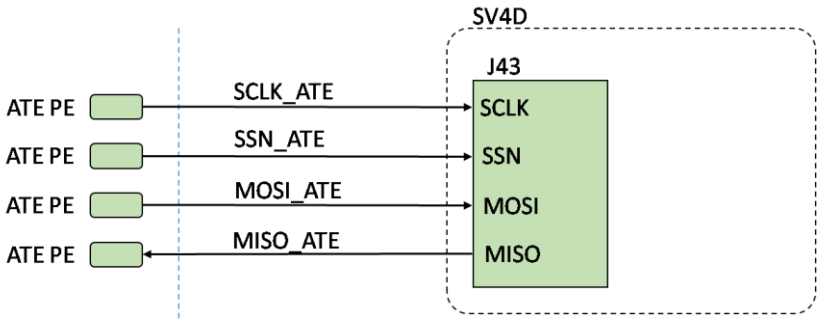


Figure 5 Simplest connection for the SPI port on SV4D

Notwithstanding the simplest SPI connection described above, it is often required to perform debugging of the register programming steps in the production test program. Such debugging can be performed using the Introspect ESP Software, and it requires enabling a USB connection to the load board. Thus, it is desirable to implement the following USB-to-SPI converter solution on the load board. It consists of a commercial FTDI module that can be socketed into the load board as well as a simple switch for selecting between the ATE pin electronics of Figure 5 and the FTDI module. In the following discussion, please refer to Figure 6 to Figure 8 below.

In Figure 6, an illustration of the FTDI FT2232H module is shown. This is a commercial module that allows for transmitting SPI commands over a USB bus connected to a PC. The module can be socketed onto the load board, and it provides two independent SPI ports that are programmed using the Introspect ESP software. In terms of implementation on the load board, Figure 7 shows the electrical connections required by the FT2232H module. As can be seen, the module receives a 5V power supply from the load board. Of the various pins available on the module, four pins are used for the SPI Port: MISO, MOSI, SSN and SCLK.

Finally, there is a pin in Figure 7 called SPI_ATE that controls a selection MUX, as shown in Figure 8. The MUX (such as that from ON Semiconductor, part number FST3257, as in this diagram) allows selection between the FT2232H module and the ATE pin electronics.

When the FT2232H module is attached and the Introspect ESP software is used, the FT2232H module will be automatically selected via the SPI_ATE pin, to drive the SPI port. Otherwise, the SPI_ATE pin is pulled high through a resistor, which selects the ATE pin electronics to drive the SPI port. The full view of the implementation is shown at the end of the document in Figure 14.

Figure 6 Illustration of the FT2232H USB-to-SPI converter module

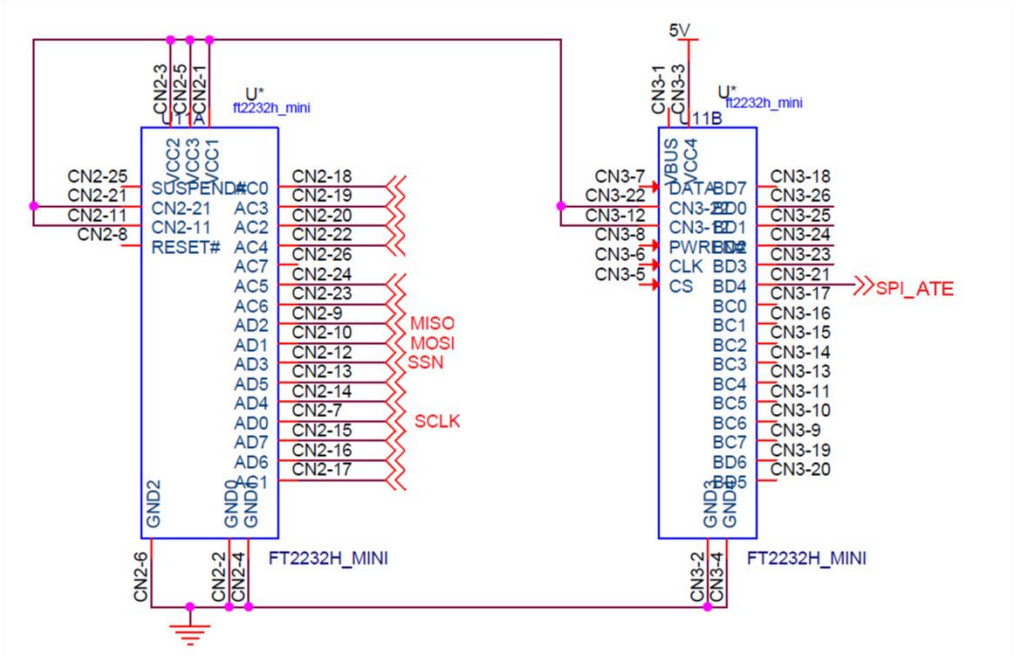


Figure 7 Schematic connections of the FT2232H module

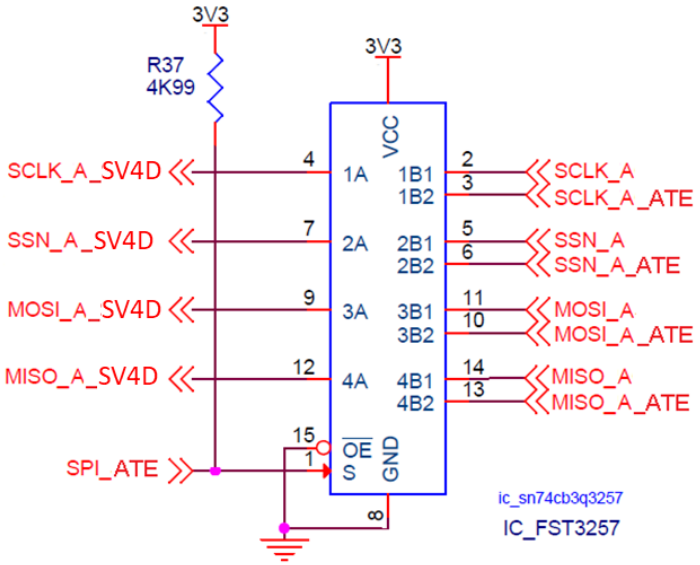


Figure 8 Schematic connections of the SPI selection switch

High-Speed Signal Connections

A conceptual illustration of the high-speed connection mechanism of the SV4D is shown in Figure 9. The module itself contains FireFly connectors, and the carrier board is expected to host corresponding ones that can be placed within 4" away from the module. This allows for optimized placement of high-speed signals relative to DUT positions. Figure 10 to Figure 13 show the schematic connections for each of the MIPI ports on the DUT carrier board.

Figure 9 Conceptual illustration of the FireFly micro flyover system

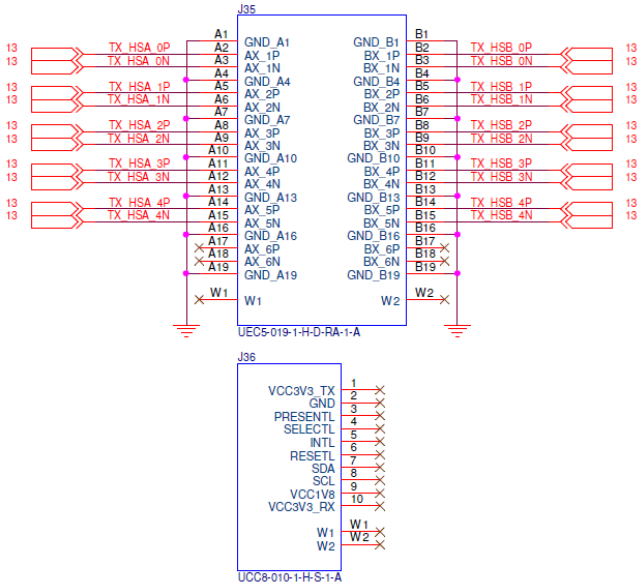


Figure 10 Schematic connections for the first pair of MIPI transmitter ports of the SV4D

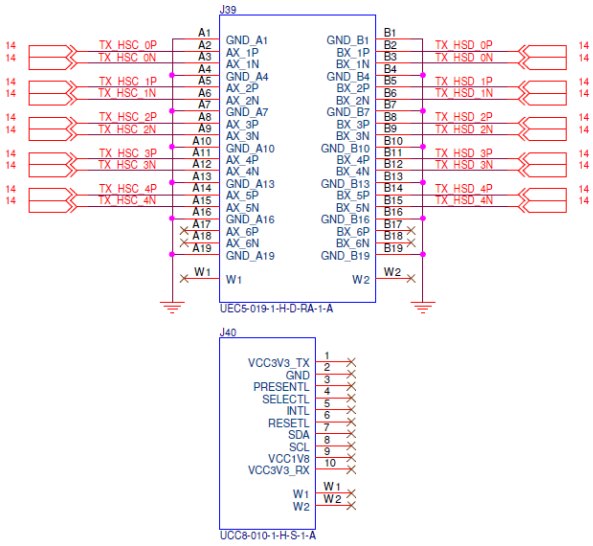


Figure 11 Schematic connections of the second pair of MIPI transmitter ports of the SV4D

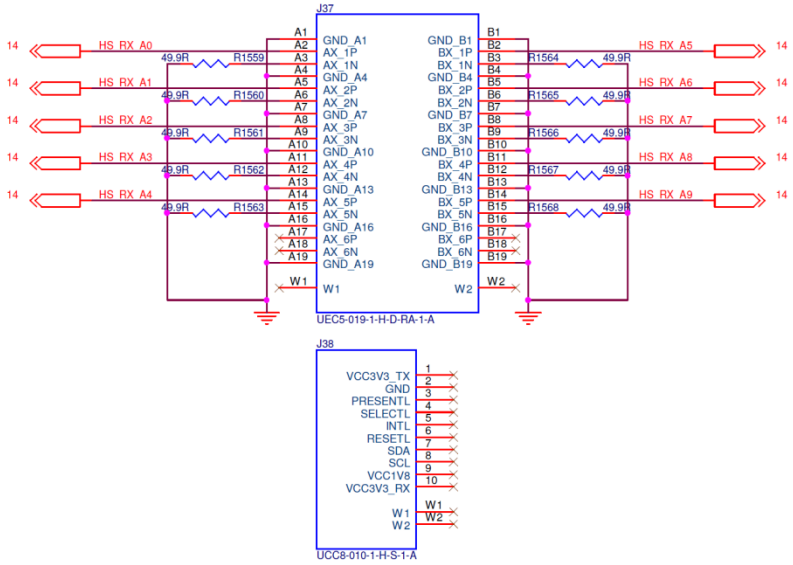


Figure 12 Schematic connections for the first MIPI receiver port of the SV4D

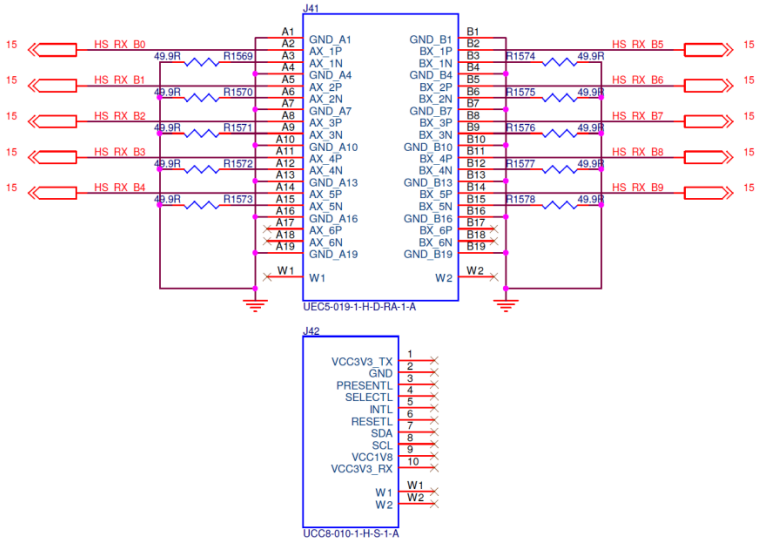


Figure 13 Schematic connections of the second MIPI receiver port of the SV4D

FULL DESIGN BLOCK DIAGRAM

A block diagram of the full SV4D implementation on a load board is shown in Figure 14. (In this case, Introspect ESP software is used to set the FST3257 MUX to select the FT2232H module SPI port, rather than the ATE SPI port).

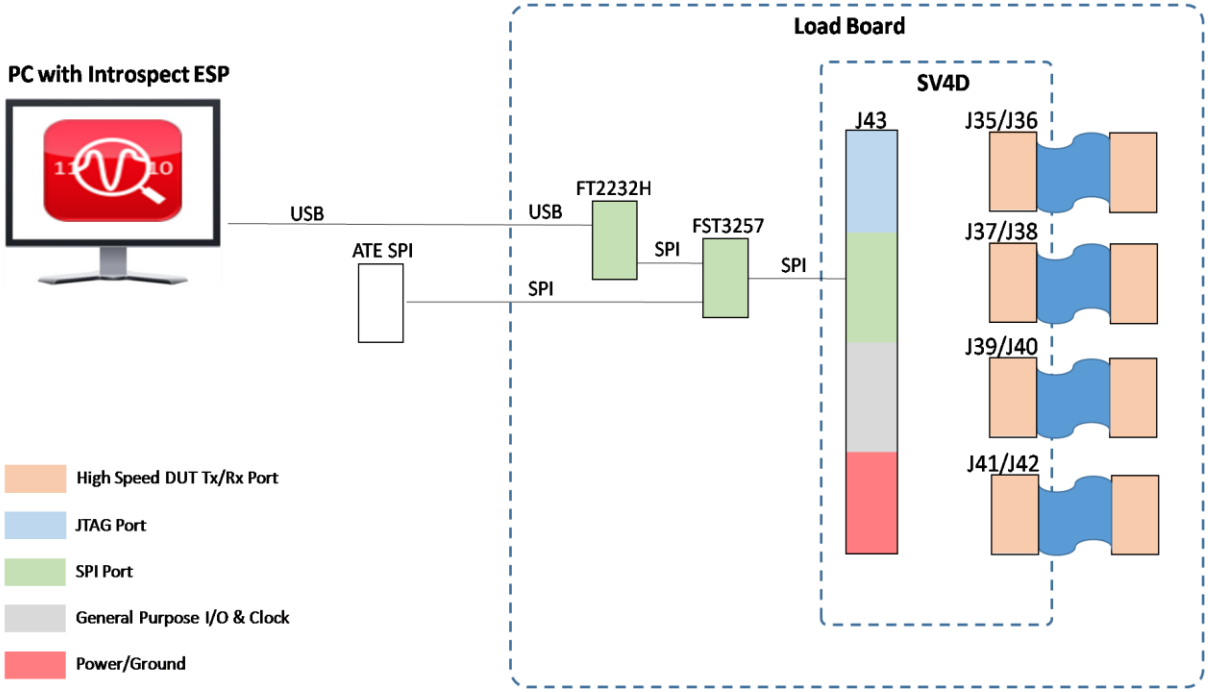


Figure 14 Block diagram of load board implementation of the SPI selection switch

Additional Documentation

SV4D Quick Start Guide: EN-G028E-E-18179 SV4D QuickStart.pdf

SV4D Command Interface Design Document: Contact Introspect Technology

SV4D Design Files.zip (includes reference schematic, layout, and CAD file for ATE load board design): Contact Introspect Technology

Revision Number	History	Date
1.0	First draft	February 8, 2018
1.1	Updated information on TX ports and SPI ports, added "Full Design Block Diagram" and "Additional Documentation" sections	October 23, 2018
1.2	Updated format, minor edits	April 9, 2019

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