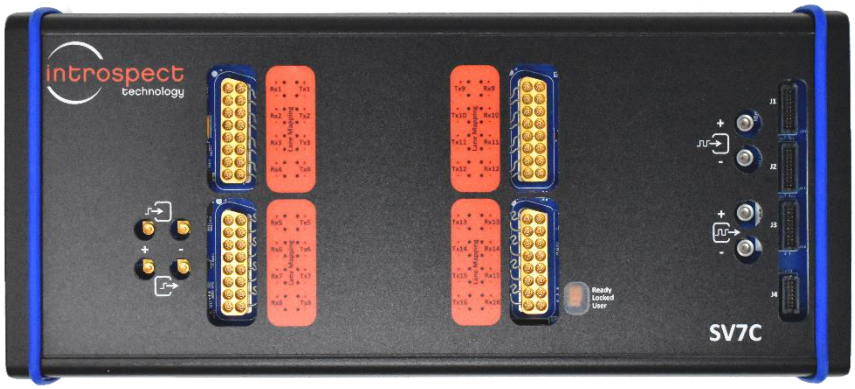
QUICK START GUIDE

Using the SV7C 32 Channel DDR Form Factor

SV7C Personalized SerDes Tester

C SERIES



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Introduction

OVERVIEW

This document describes the required steps for combining two SV7C devices into a single, unified form factor. This form factor, SV7C_32C16G_DDR, is a superset of the SV7C_16C17G_DDR form factor and provides 32 phase aligned transmitter channels. The hardware requirements are given below.

IMPORTANT NOTE

The SV7C_32C17G_DDR form factor is to be used with 2 SV7C boxes only. In the case of a bidirectional kit (BDK) being included, another form factor will be used. This form factor can be set up the same way as the SV7C_32C17G_DDR form factor.

REQUIREMENTS

- (QTY = 2) - SV7C Personalized SerDes Tester (power supplies and USB cables included)
- (QTY = 2) - 12-inch phase-matched cables, SMP female to SMP female (manufacturer part number Amphenol SV Microwave 7012-1292, or contact Introspect)
- (QTY = 2) - 12-inch MMPX to MMPX cable 12 inch (Huber+Suhner MF86/11MMPX/11MMPX /305mm)
- (QTY = 1) - 8-wire 14-pin to 14-pin GPIO cable (Samtec SFSDT-07-28-G-08.00-DR-NDX)

IMPORTANT NOTE

For fully phase aligned operation across all 32 TX channels, a calibration must be performed on the two SV7C modules. This calibration may be performed in the factory before shipment of a pair of units, or it may be performed "in-field". Please refer to the document "EN-G034E-E-24159 SV7C In-Field Calibration Scripts" for in-field calibration instructions.

Step by Step Guide

CUSTOM FORM FACTOR CREATION

1. Add the provided custom form factor JSON file to the following location:

   `<path>/Introspect/Config/customFormFactors/SV7C_32C17G_DDR.json`

2. Open the Pinetree software with the SV7C_16C17G_DDR form factor, as below:

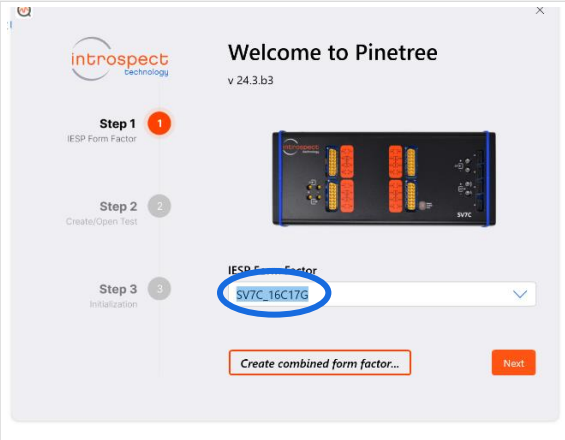

Figure 1: Screen capture of the GUI and choosing the SV7C_32C17G_DDR form factor.

3. Connect the USB cable from your PC to the first SV7C (referred to here as "Box 1"). After connecting to Box 1 via the Pinetree software (IESP/SV7C_16C17G_DDR -> Connect), you will see serial numbers in the log, like those shown below:

```
Connecting to serialNum 'FTDI:INSV7C230309A'
Connected to subPart 'SV7C_16C17G_DDR_A'
Connecting to serialNum 'FTDI:INSV7C230309B'
Initializing IESP hardware/firmware
Doing post-connection initialization
```

4. Connect the USB cables from your PC to both SV7C boxes and open the GUI with the SV7C_32C17G_DDR form factor.

5. Open the "ConnectionConfig" tool (IESP/SV7C_32C17G_DDR -> ConnectionConfig). Select the FtdiSerialNumber for box 1 to be the number recorded in step 2, and use the other option in the drop-down menu for box 2, as shown below:

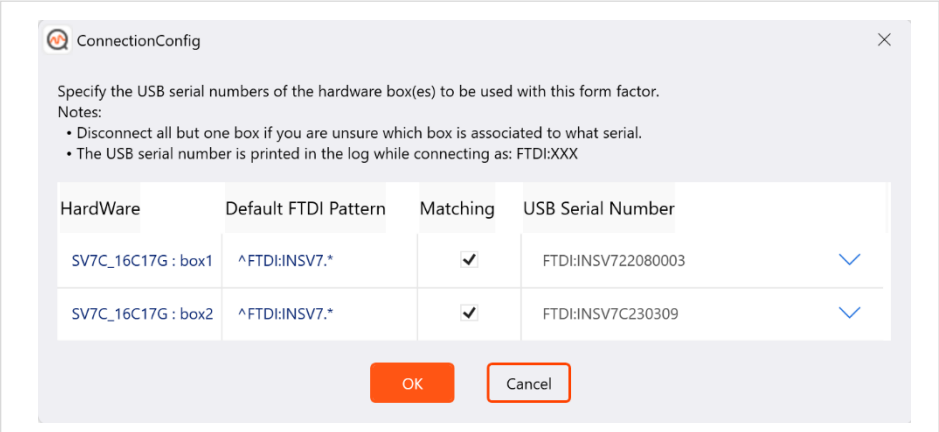

Figure 2: Screen capture showing the "ConnectionConfig" tool.

6. Close the "ConnectionConfig" tool and connect to both SV7C boxes (IESP/SV7C_32C17G_DDR -> Connect). You should see a successful connection to both boxes like below.

```
Connecting to serialNum 'FTDI:INSV7C22080003A'
Connected to subPart 'SV7C_16C17G_DDR_box1_A'
Connecting to serialNum 'FTDI:INSV7C22080003B'
Connecting to serialNum 'FTDI:INSV7C230309A'
Connected to subPart 'SV7C_16C17G_DDR_box2_A'
Connecting to serialNum 'FTDI:INSV7C230309B'
Initializing IESP hardware/firmware
Doing post-connection initialization
```

SV7C CONNECTION DIAGRAMS

Diagrams showing the required connections of the two modules are given in the figure below. Figure 3 shows the full set of cable connections between Box 1 and Box 2. In addition to the reference clock connections, there are three sets of cable connections. Refer to Table 1 for the GPIO connection.

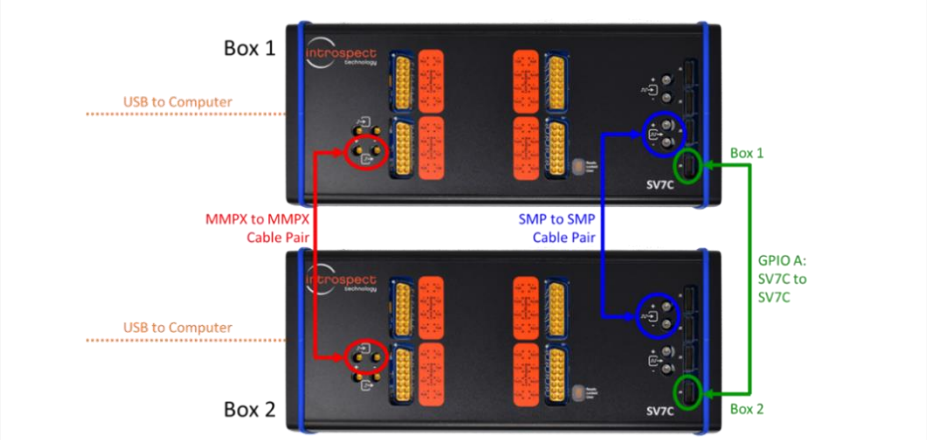

Figure 3: Block diagram of required cable connections between SV7C modules.

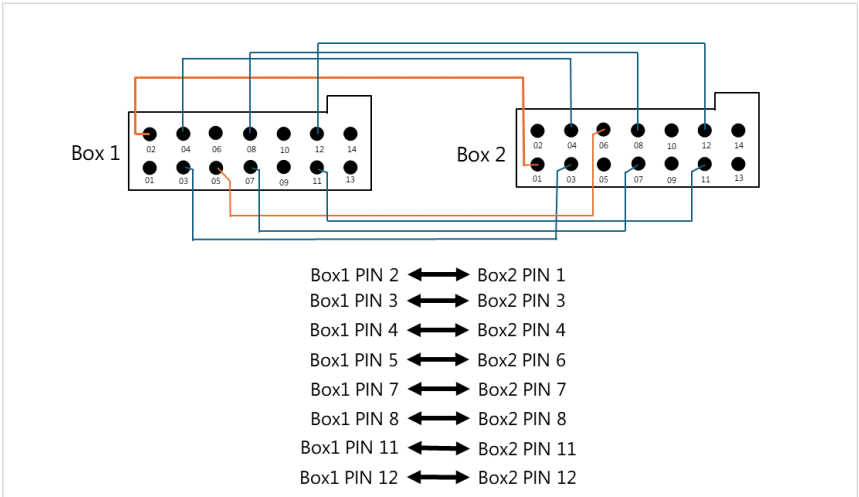

Figure 4: GPIO pin connections.

USING THE SV7C_32C17G_DDR FORM FACTOR

Open a new test procedure with the SV7C_32C17G_DDR form factor. In the new form factor, under globalClockConfig, you will see that two "referenceClocksConfig" components have automatically been created. This is as shown in the screen capture in Figure 4.

Note that the "refClocksConfig1" component controls "Box 1" and has been configured to use its internal "systemRefClockSource" while the "refClocksConfig2" component controls "Box 2" and has been configured to use an external reference clock provided by "Box 1". This matches the cable setup as shown in Figure 3.

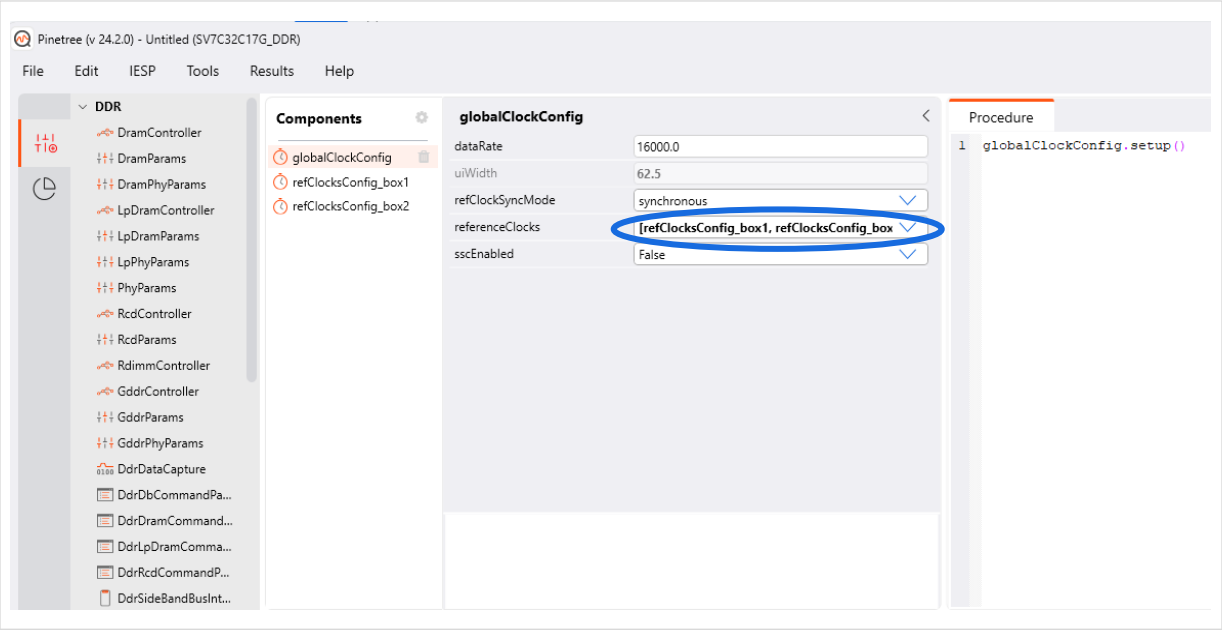

Figure 5: Screen capture showing two "referenceClocksConfig" components automatically created.

Under the "components" windowpane, press "Add" and add a "txChannelList" component. Once added, you may change the number of channels to the full range of 1-32. This is as shown in the screen capture in Figure 5. Note that channels 1-16 are on "Box 1", and channels 17-32 are on "Box 2".

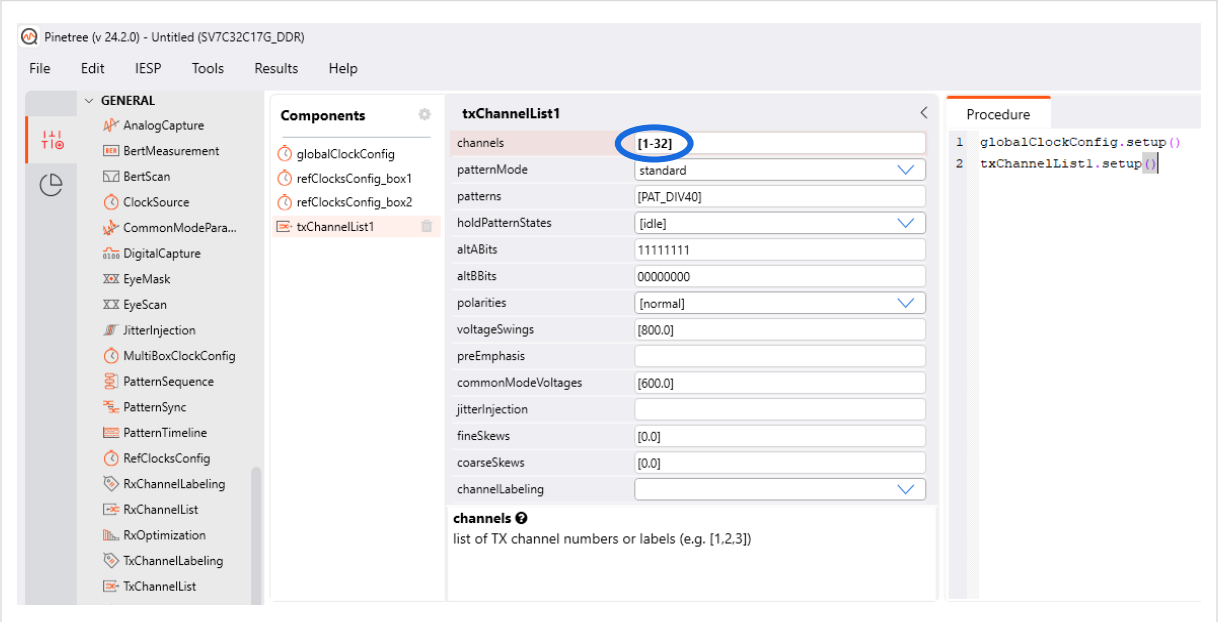

Figure 6: Changing the number of channels to the full range of 1-32.

All other operations for the form factor SV7C_32C17G_DDR may be used as in the previous 16 channel form factor. Existing test procedures developed for the 16-channel form factor may be imported and channel lists modified as required.

IMPORTANT NOTE

If phase alignment across all 32 TX channels has been performed as in in-field calibration (see the document "EN-G034E-E-24159 SV7C In-Field Calibration Scripts") then it is important to externally label the first SV7C unit (master) as "Box 1" and the second unit (slave) as "Box 2". This labelling must be kept consistent during subsequent usage. TX Channels 1-32, as shown in the channel list above, will not be aligned if the order of Box 1 and Box 2 is changed.

REVISION NUMBER	HISTORY	DATE
1.0	Document release	June 7, 2024
1.1	Updated pin numbering in Figure 4	July 16, 2024

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