SV4D Direct Attach MIPI Test Module

Data Sheet

VERSION 1.0

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INTRODUCTION

Overview

The SV4D Direct Attach MIPI Test Module is the latest member of the Introspect Technology D-Series, targeting the mass production test of semiconductor devices based on MIPI® Alliances interfaces. This ultra-compact test module enables at-speed production testing from wafer sort all the way through to production final test. The module has been designed to be readily integrated on any ATE load board or DIB with minimal external components, and supports multi-port, multi-site testing with configurable protocol support for MIPI CSI-2SM, DSISM, and DSI-2SM. The SV4D is ideal for high-end applications such as camera and image sensors, apps processors, SOC, and DDIC. Coupled with an exceptionally powerful software development environment, the SV4D provides the fastest path for MIPI mass production test.

Key Benefits

- Four complete D-PHYSM transmitters on one module[1], with operation up to 2.5 Gbps
- Two complete C-PHYSM or D-PHY receivers on one module[1], with operation up to 2.5 Gsps/Gbps
- Support for MIPI DSI, DSI-2, and CSI-2 protocols
- Coverage for sLVDS or LVCMOS test applications
- State of the art programming environment based on the highly intuitive Python language
- Multi-site test capability, tiny footprint and minimal I/O requirements

[1]The SV4D is licensed either as a transmitter tester or a receiver tester.

Applications

- Production testing of display driver ICs
- Production testing of image sensors
- Production testing of connectivity and bridge devices
- Production testing of FPGAs, AI co-processors, and microcontrollers

SV4D Ordering Information

This product is part of a family of MIPI generator and receiver products. The following table describes the part numbers and key feature differentiators.

Table 1 Ordering part numbers for this product and related ones.

Part Number	Name	Key Differentiators
6202	**SV4D DPTX**	SV4D Module with transmitter firmware
6204	**SV4D CPRX / SV4D DPRX**	SV4D module with receiver firmware
6280	**SV4M**	Carrier Board for SV4D

Related Documents

- EN-G029E-E-19099 - SV4D Reference Design Guide.pdf
- EN-G031E-E-19081 - SV4D Quick Start Manual
- EN-G032E-E-19081 - SPI Communications Overview
- SV4D Design Files.zip (includes reference schematic, layout, and CAD file for ATE load board design)

FEATURES

Block Diagram

A high-level block diagram of the SV4D MIPI Test Module is shown in Figure 1 All SV4D pins natively support LP and HS signalling.

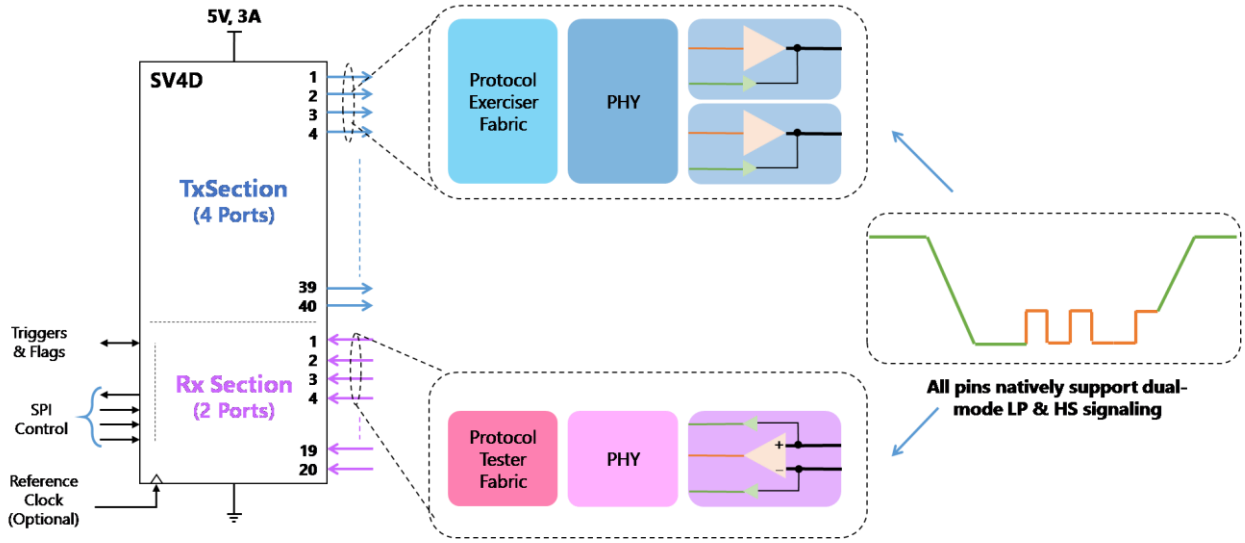
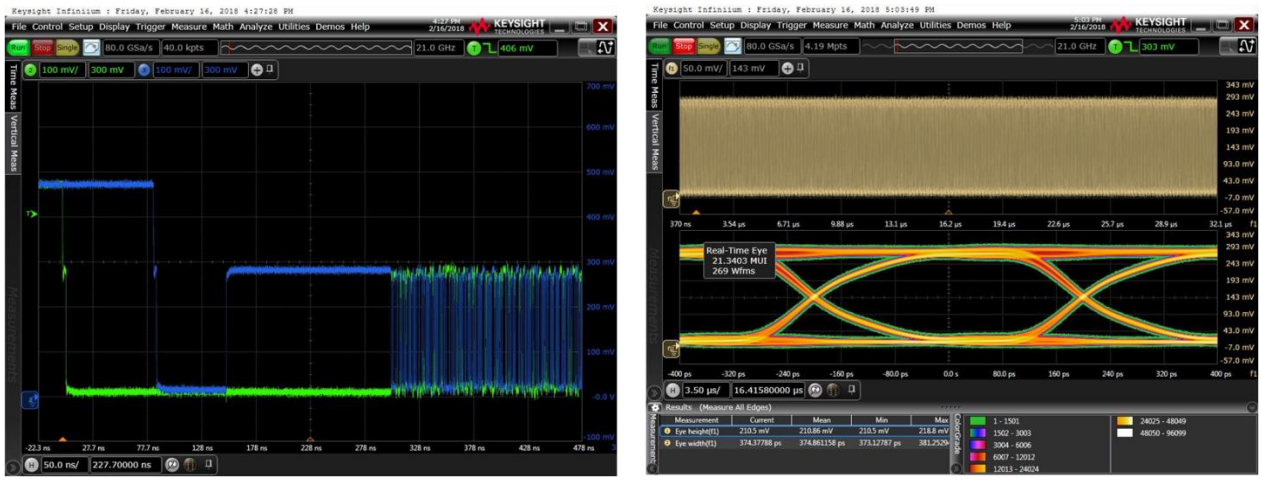


Figure 1 High level block diagram of the SV4D MIPI Test Module

DPHY Transmitter

The **SV4D DPTX** builds on Introspect's existing data rate synthesis technology. its capable of maintaining clock and data alignment at any rate from 156.25 Mbps to 2.5 Gbps. The SV4D DPTX offers fully integrated LP pattern generation and per-lane HS amplitude control.



(a) *(b)*

Figure 2 SV4D DPTX waveforms: (a) measured LP-HS transition (b) measured HS eye opening at 2.5 Gbps

Combined DPHY / CPHY Receiver

The **SV4D DPRX / CPRX** provides the unique ability to be configured for either D-PHY or C-PHY testing, operating in a data rate range of 156.25 Mbps/Msps to a maximum of 2.5 Gbps/Gsps. Each receiver also provides automatic dynamic receiver termination on detection of LP ->HS ->LP transitions. Figure 3 below shows a high-impedance, differential waveform at the SV4D RX input explicitly showing the 100 ohm differential receiver termination turning onafter an LP11 to LP00 transition is detected.

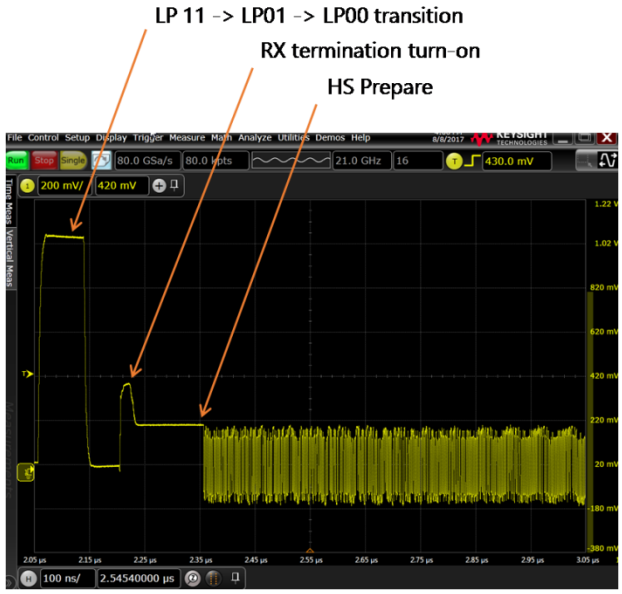


Figure 3 SV4D Receiver Waveform: Measurement demonstrating SV4D automatic termination detection

Physical Layer Production Test

The **SV4D DPTX** allows for the creation of realistic stimulus conditions including key MIPI D-PHY timing parameters associated with HS-entry and HS-exit transitions. Typical waveforms are shown below in Figure 4. A list of key timing parameters which can be controlled by the SV4D is given in Table 2. In addition to the listed timing parameters, bit definitions such as SOT, HsZero and HsTrail, ClkZero and ClkTrail can be programmed through the GUI as required.

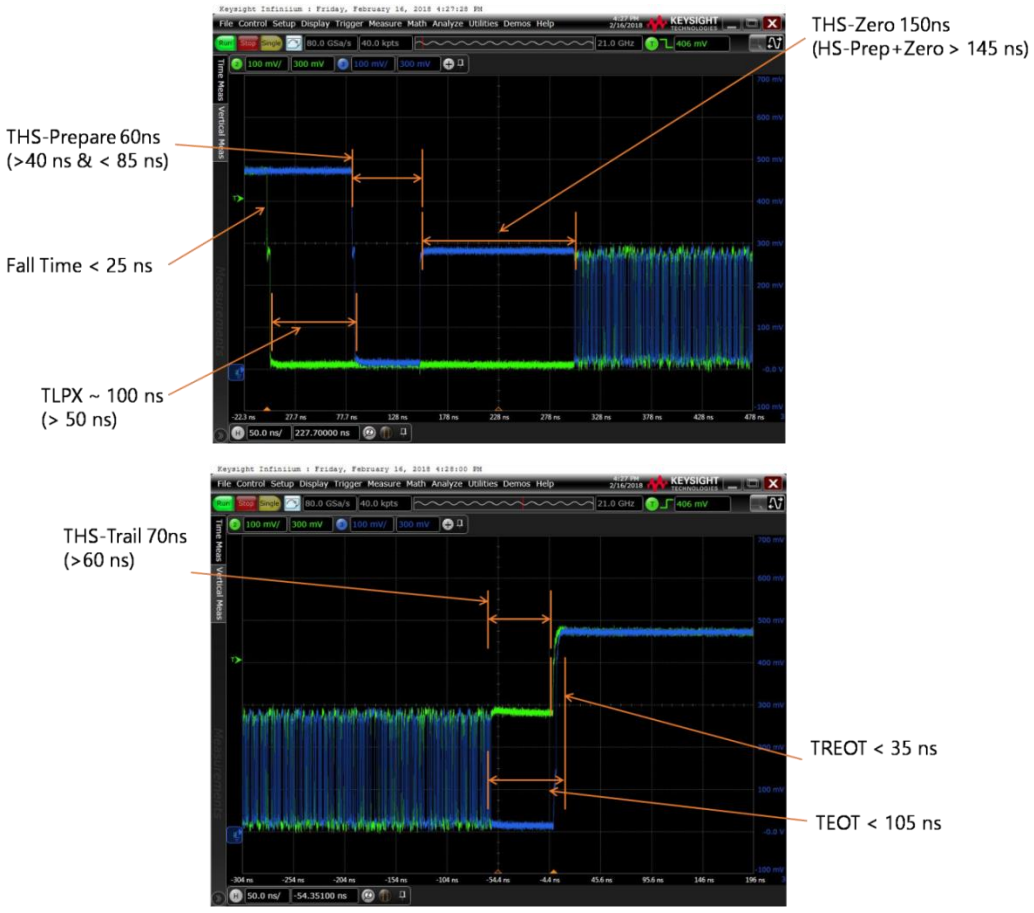


Figure 4 Typical SV4D DPTX HS Entry and HS Exit waveforms at 2.5 Gbps

Table 2 Key MIPI timing parameters controlled by SV4D DPTX

Parameter Type		**Timing parameter controls provided by SV4D**
Hs Entry	Clock	$T_{CLK-LPX}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$,
	Data	T_{LPX}, $T_{HS-PREPARE}$, $T_{HS-ZERO}$
Hs Exit	Clock	$T_{CLK-TRAIL}$, $T_{CLK-POST}$
	Data	$T_{HS-TRAIL}$, $T_{HS-EXIT}$

The **SV4D DPRX / CPRX** allows for physical layer measurements such as BER testing on received packets, as illustrated in Figure 5. As outlined in the diagram, a series of triggered BERT measurements may be performed on received HS data. BERT measurements begin only after specified LP sequences are received, and BERT measurements begin only after a SOT or Sync word is successfully received in each packet on each lane or Trio.

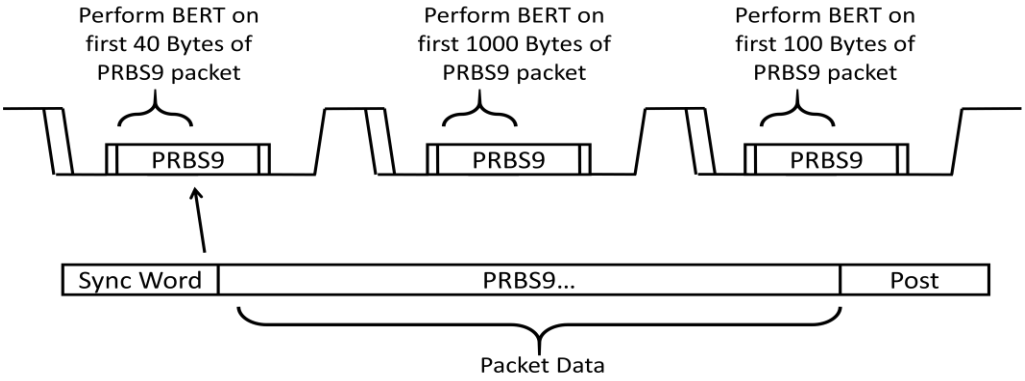


Figure 5 BER test capabilities with received HS data packets

Protocol Layer Production Test

The SV4D is capable of transmitting and receiving complete **CSI-2 or DSI-2** frames and video. As such, the SV4D may be used as an emulator for either cameras or display devices, which makes the SV4D particularly useful in the rapid screening, calibration, and final test for complete systems. See the following Software Automation section below for an overview of SV4D DPTX functionality.

Software Automation

The SV4D is operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shots in Figure 6. Component-based design is Introspect ESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. Also note that the software supports the automatic generation of SPI test vectors which can be imported into an ATE environment. Further details of the features shown in the figure and support for ATE integration are given in the SV4D DPTX Quick Start Manual.

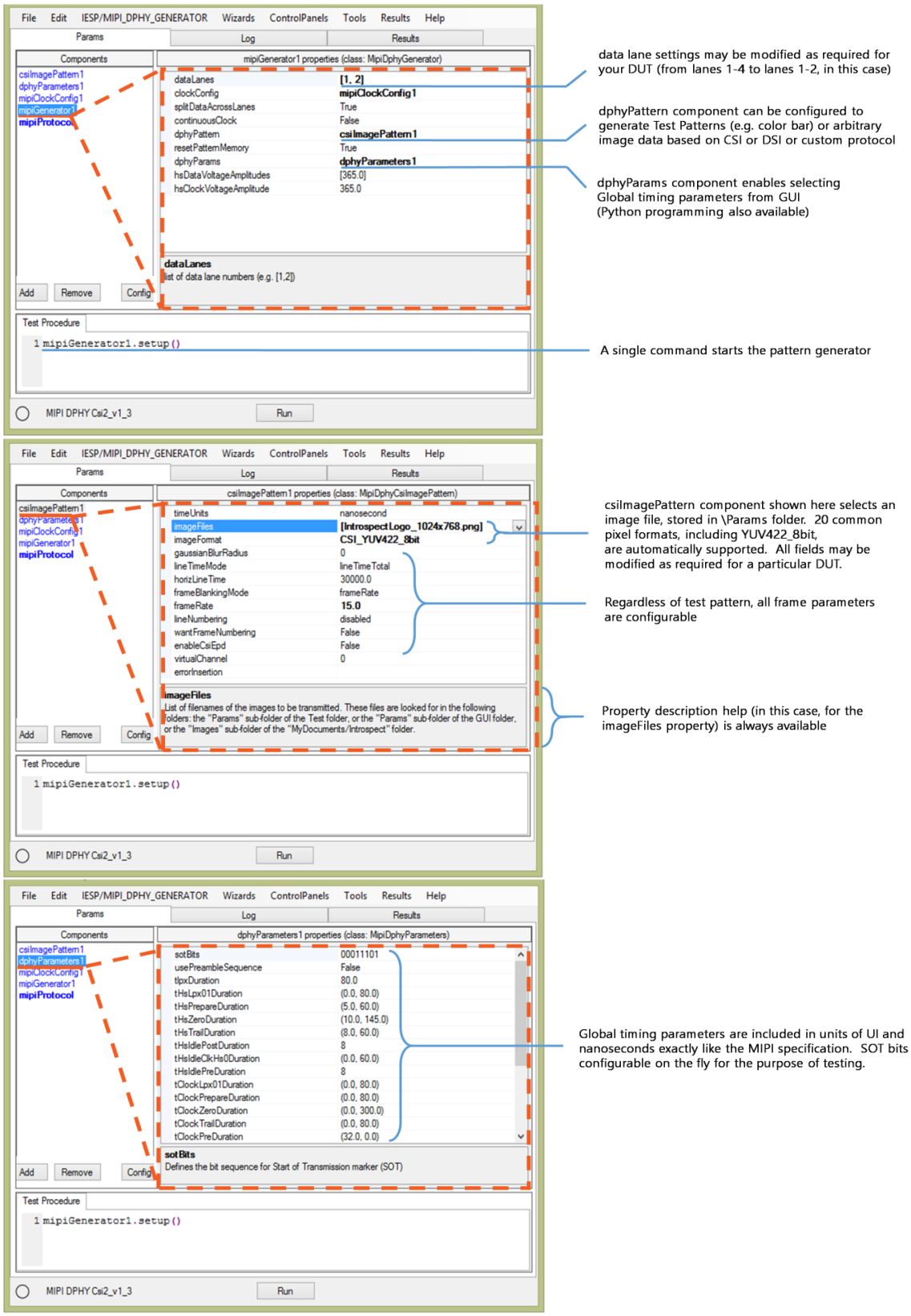


Figure 6 The Introspect component based software environment (a) MIPI generator top level component (b) CSI-2 frame generation with MIPI pattern component (c) Precise timing with the parameter component

Triggers, Flags, and General Purpose I/O

The SV4D provides a set of general purpose I/O signals that can be used for implementing custom vector programming or specialized functions. This includes two trigger pins (input to the SV4D), two flag pins (output from the SV4D), and seven GPIO (can be designated as either input or output and assigned custom functions in firmware). All I/O pins are 1.8 V LVCMOS compatible, and the detailed pinout of these 11 pins is providedinTable 7.

Input Reference Clock

The SV4D also allows for direct synchronization with an external input reference clock. The input frequency range is from 10 to 250 MHz. The intended clock interface is 1.8 to 3.3 V LVDS, but it is also possible to drive this SV4D reference clock with single ended CMOS signal. Please see the reference design guide, "EN-G029E-E-19074 - SV4D Reference Design Guide.pdf" for additional implementation details.

SPI Communications Port

The SV4D is controlled by a single SPI port facilitating register reads and writes to the real-time operating system in the module. The maximum speed of the SPI bus is 6 MHz, and it is compatible with 1.8 V LVCMOS logic. Please see the document "SPI Communications Overview" for full timing details and see Table 7 for the pinout of the four required connections (SPI_SSN, SPI_CLK, SPI_MOSI, and SPI_MISO) for the SPI bus.

The SPI bus operates in a master / slave arrangement, with the Master being either (1) the controlling PC (connected to the module via the SV4D Carrier Board) via the Introspect ESP software, or (2) the ATE (connected to the module via the ATE load board). The SV4D module always operates as the SPI slave. Please see the "EN-G029E-E-19074 - SV4D Reference Design Guide.pdf" for further load board implementation details.

JTAG Port

The JTAG port is used for loading firmware updates to the SV4D module. Firmware updates are provided seamlessly using the SV4D Carrier Board, as part of the design kit. Please refer to the User Manual, "EN-G028E-E-19074 - SV4D Quick Start Guide" for further details and see Table 7 for the listing of the JTAG pins (TMS, TCK, TDO, TDI).

CONNECTORS AND PIN OUT

Figure 7 shows a photograph of the top and bottom sides of the SV4D with each of its ports and connectors. The physical area of the SV4D is 3" by 3" (76 mm by 76 mm). The SV4D is mounted on the load board using a single mezzanine connector(J43). High-speed signals are transmitted over miniature board-to-cable assemblies.

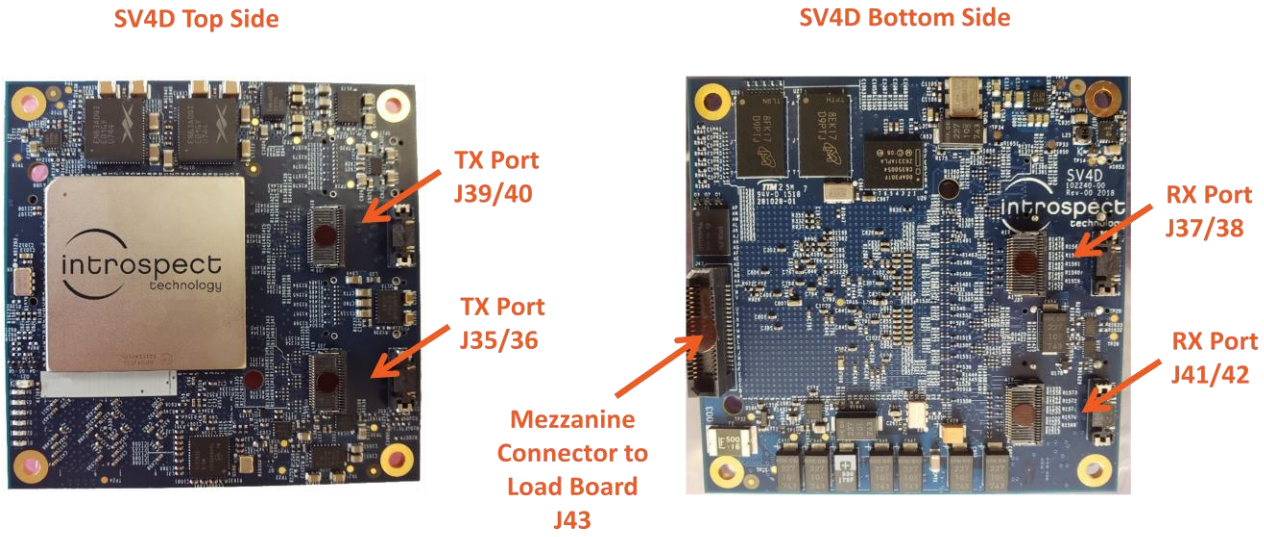


Figure 7 Connectors on top and bottom of the SV4D board

The pinouts for each of the five connectors (two TX ports, two RX ports, and one lower speed mezzanine connector which connects to the load board) as shown above are each provided in the following five tables.

Additional descriptions of the lower speed signals on J43 can be found in the SV4D Reference Design Guide (see listing of additional documents Additional information on the connector footprints can be found on the Samtec website at the links preceding each table:

J35, J37, J39, J41: Samtec Part number UEC5-019-1-H-D-RA-1-A,
https://www.samtec.com/products/ucc8-010-1-h-s-1-a

J36, J38, J40, J42: Samtec Part Number UCC8-010-1-H-S-1-A
https://www.samtec.com/products/uec5-019-1-h-d-ra-1-a

Mating Firefly Cable Assemblies:
https://www.samtec.com/products/ecue

- Note: please use the cables provided by Introspect or ensure 1:1 pin mapping in cable assemblies to match SV4D to load board pinouts.

Table 3 Signal mapping for SV4D TX Port A and B, J35/J36

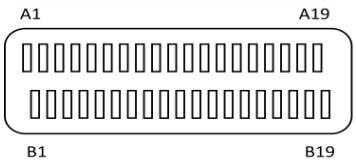
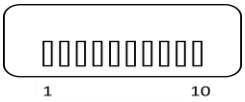
Footprint	PORT A		PORT B	
	Pin Number	DPHY TX Signal	Pin Number	DPHY TX Signal
J35 Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J35, A2	Data 0, P	J35, B2	Data 0, P
	J35, A3	Data 0, N	J35, B3	Data 0, N
	J35, A5	Data 1, P	J35, B5	Data 1, P
	J35, A6	Data 1, N	J35, B6	Data 1, N
	J35, A8	Data 2, P	J35, B8	Data 2, P
	J35, A9	Data 2, N	J35, B9	Data 2, N
	J35, A11	Data 3, P	J35, B11	Data 3, P
	J35, A12	Data 3, N	J35, B12	Data 3, N
	J35, A14	CLK, P	J35, B14	CLK, P
	J35, A15	CLK, N	J35, B15	CLK, N
J36 Part Number: SamtecUCC8-010-1-H-D-S-1-A  	J36	No Connections (required part, must be mounted for mechanical reasons)	J36	No Connections (required part, must be mounted for mechanical reasons)

Table 4 Signal mapping for SV4D TX Port C and D, J39/J40

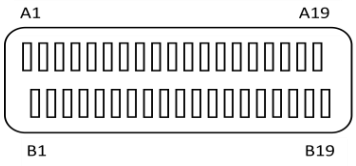
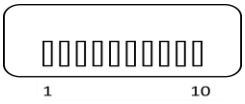
Footprint	PORT C		PORT D	
	Pin Number	DPHY TX Signal	Pin Number	DPHY TX Signal
J39 Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J39, A2	Data 0, P	J39, B2	Data 0, P
	J39, A3	Data 0, N	J39, B3	Data 0, N
	J39, A5	Data 1, P	J39, B5	Data 1, P
	J39, A6	Data 1, N	J39, B6	Data 1, N
	J39, A8	Data 2, P	J39, B8	Data 2, P
	J39, A9	Data 2, N	J39, B9	Data 2, N
	J39, A11	Data 3, P	J39, B11	Data 3, P
	J39, A12	Data 3, N	J39, B12	Data 3, N
	J39, A14	CLK, P	J39, B14	CLK, P
	J39, A15	CLK, N	J39, B15	CLK, N
J40 Part Number: SamtecUCC8-010-1-H-D-S-1-A  	J40	No Connections (required part, must be mounted for mechanical reasons)	J40	No Connections (required part, must be mounted for mechanical reasons)

Table 5 Signal mapping for SV4D RX Port A, J37/J38

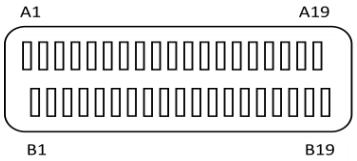
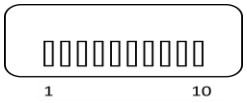
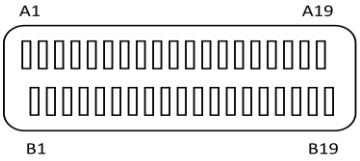
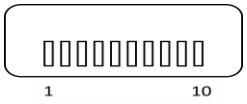
Footprint	Pin Number	PORT A CPHY RX Signal	DPHY RX Signal
J37 Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J37, A2 J37, A5 J37, A8 J37, A11 J37, A14 J37, B2 J37, B5 J37, B8 J37, B11 J37, B14	Trio 0, A Trio 0, B Trio 0, C Trio 1, A Trio 1, B Trio 1, C Trio 2, A Trio 2, B Trio 2, C No Connection	Data 0, P Data 0, N Data 1, P Data 1, N Data 2, P Data 2, N Data 3, P Data 3, N CLK, P CLK, N
J38 Part Number: SamtecUCC8-010-1-H-D-S-1-A  	J38	No Connections (required part, must be mounted for mechanical reasons)	No Connections (required part, must be mounted for mechanical reasons)

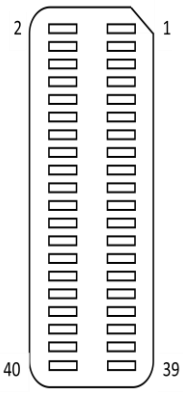
Table 6 Signal mapping for SV4D RX Port B, J41/J42

Footprint	Pin Number	PORT B CPHY RX Signal	DPHY RX Signal
J41Part Number: Samtec UEC5-019-1-X-D-RA-1-A  	J41, A2 J41, A5 J41, A8 J41, A11 J41, A14 J41, B2 J41, B5 J41, B8 J41, B11 J41, B14	Trio 0, A Trio 0, B Trio 0, C Trio 1, A Trio 1, B Trio 1, C Trio 2, A Trio 2, B Trio 2, C No Connection	Data 0, P Data 0, N Data 1, P Data 1, N Data 2, P Data 2, N Data 3, P Data 3, N CLK, P CLK, N
J42Part Number: SamtecUCC8-010-1-H-D-S-1-A  	J42	No Connections (required part, must be mounted for mechanical reasons)	No Connections (required part, must be mounted for mechanical reasons)

J43: Samtec Part Number ERF8-020-07.0-S-DV-K-TR
https://www.samtec.com/products/erf8-020-07.0-s-dv-k-tr

Mating connector to J43: ERM8-020-05.0-S-DV-K-TR
https://www.samtec.com/products/erm8-020-05.0-s-dv-k-tr

Table 7 Signal mapping for SV4D Low Speed Connector, J43

Footprint	Pin	Signal Name	Pin	Signal Name
	**1**	GND	21	FLAG1
	2	JTAG TMS	22	FLAG0
	3	GND	23	TRIG1
	4	JTAG TCK	24	TRIG0
	5	GND	25	SEQUENCE ON
	6	JTAG TDO	26	GPIO6
	7	GND	27	GPIO5
	8	JTAG TDI	28	GPIO4
	9	GND	29	VIN (5V)
	10	SPI SSN	30	GPIO3
	11	GND	31	VIN (5V)
	12	SPI SCLK	32	GPIO2
	13	GND	33	VIN (5V)
	14	SPI MISO	34	GPIO1
	15	VIN (5V)	35	VIN (5V)
	16	SPI MOSI	36	GPIO0
	17	VIN (5V)	37	GND
	18	RESET_N	38	CLKIN P
	19	VIN (5V)	39	GND
	20	READY	40	CLKIN N

For the low-speed connector above, all GPIOs operate at 1.8V LVCMOS.

The SV4D also allows for synchronization with an external input reference clock. The CLKIN P and CLKIN N pins are designed to interface to 1.8 to 3.3 V LVDS, but may be connected to single-ended LVCMOS if the CLKIN N is connected directly to ground.

PHYSICAL DIMENSIONS

Figure 8 and Figure 9 below shows the mechanical dimensions for the top and bottom of the SV4D board in further design detail.

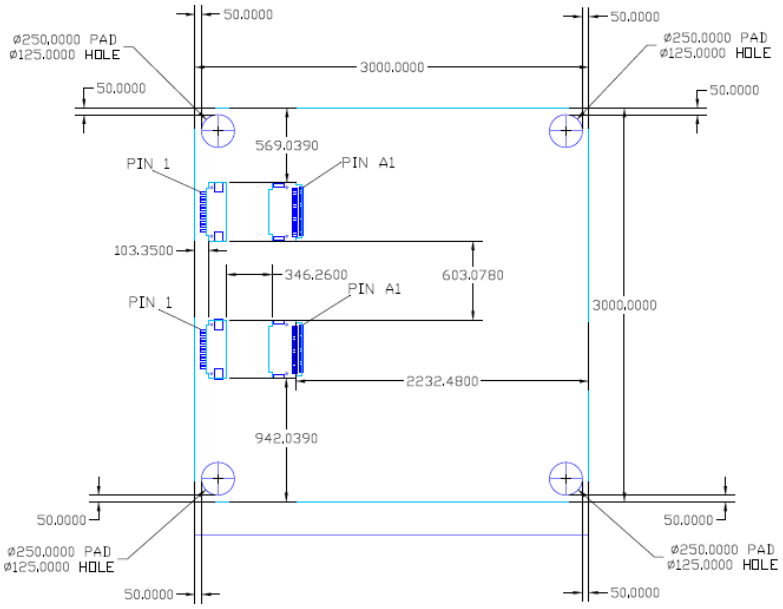


Figure 8 Top view of SV4D module. Measurements are in mil

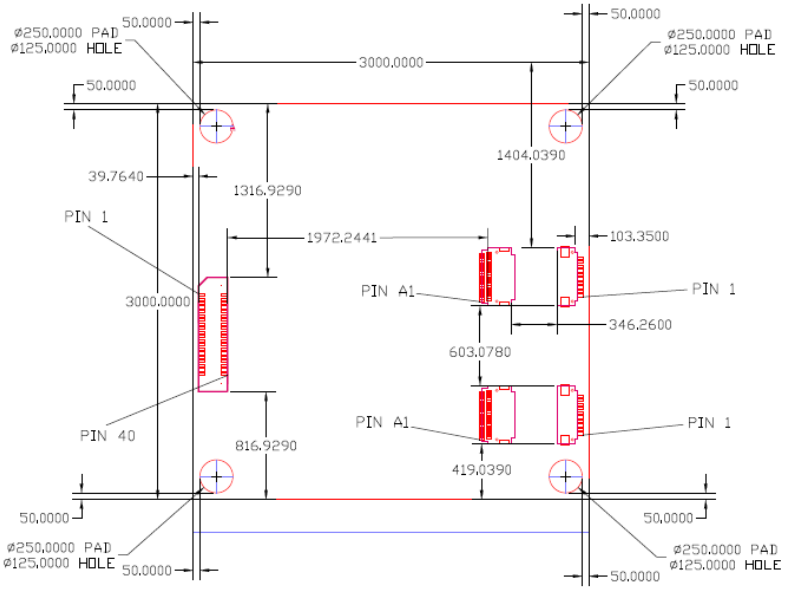


Figure 9 Bottom view of SV4D module. Measurements are in mil

SPECIFICATIONS

Table 8 General Specifications

Parameter	Value	Units	Description and Conditions
Application / Protocol Support			
Physical layer interface			
Transmitters:	D-PHY, CSI/DSI		Flexible pattern architecture allows for the generation of encoded PHY data, unencoded PHY data, or entire CSI/DSI frames
Receivers	D-PHY, CPHY, CSI/DSI		
Compression protocol	VESA DSC v1.2		
LP/HS handling	Automatic		Tester automatically generates LP and HS data
Ports			
Number of transmitter ports	4		
Maximum number of lanes per port	4 Data + 1 Clock		
Number of receiver ports	2		
Maximum number of lanes per port	4 Data + 1 Clock		
Number of external reference clock Inputs	1		Used as external reference for synchronization
Number of GPIO Pins	7		Used for executing pattern vectors
Number of Trigger Input Pins	2		Armed in software for triggering fast pattern starts in production testing
Number of Flag Output Pins	2		Armed in software to flag test completion or pass/fail criteria available on request
Data Rates and Frequencies			
Minimum Data Rate	156.25	Mbps	
Maximum Data Rate	2.5	Gbps	
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Maximum GPIO clock frequency	10	MHz	
Minimum LP State Period	25	ns	LP period is an integer multiple of HS period. Compiler automatically selects period to satisfy MIPI specification
Maximum LP State Period	240	ns	LP period is an integer multiple of HS period

Table 9 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
HS Output Coupling			
HS output single ended impedance	50 +/- 5	Ω	Automatically switchable based on HS-entry sequence
	Hi-Z	Ω	Automatically switchable based on HS-entry sequence
Termination switch time resolution	10	ns	Default termination switching time is set to be compliant with MIPI D-PHY global timing parameters
LP output single-ended impedance	> 100	Ω	Impedance when driving LP Data
	Hi-Z	Ω	Impedance when receiving BTA response data (bi-directional)
HS Voltage Performance			
Minimum single-ended output voltage swing	150	mV	Peak-to-peak specification
Maximum single-ended output voltage	360	mV	
Voltage programming resolution	10	mV	
Rise and Fall Time	120	ps	Typical
Level Setting	Per-Lane		
HS Jitter Performance			
Random Jitter Noise Floor	1.5	ps	This is an RMS RJ number
Deterministic Jitter Noise floor	TBD	ps	This is a peak-to-peak number
Timing Generator Performance			
Resolution at maximum data rate	250	mUI	
Differential non-linearity error	+/- 0.5	LSB	
Integral non-linearity error	+/- 5	ps	
LP Voltage Performance			
LP logic high level	1.2	V	
LP logic low level	0	mV	

Table 10 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
Input Impedance	50 +/- 5 Hi-Z	Ω Ω	
HS Voltage Threshold			
Minimum Detectable Differential Voltage	90	mV	Specified as 2 x 45 mV single-ended |VOD| described in C-PHY
Maximum Allowable Differential Voltage	500	mV	
HS Timing Generator Performance			
Resolution at Maximum Data Rate	7.8125	mUI	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	+/- 2	UI	
LP Voltage Threshold			
Threshold Voltage	600	mV	

Table 11 Pattern and Protocol Handling Characteristics

Parameter	Value	Units	Description and Conditions
User-programmable Pattern Memory			
Individual Expected Pattern	Per-lane		
Minimum Pattern Segment Size	8	bits	
Maximum Pattern Segment Size	512	MBytes	
Total Memory Space for Transmitters	512	Mbytes	
BERT Characteristics			
Maximum Packet Size	$2^{32} - 1$		
Maximum Number of Packets	$2^{32} - 1$		
Maximum Number of Repeats	$2^{32} - 1$		
Maximum Time Between SOT in Burst Mode	1	ms	
Capture Memory Depth	512	MBytes	

Table 12 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	Kbps	

Table 13 Software Environment and Mechanical Characteristics

Parameter	Value	Units	Description and Conditions
OS Support			
Windows 7, 8, 10	Supported		
Communications Interface			
ATE Vector Bus	Supported		
DC Power			
Supply Voltage	5	V	
Dimensions			
Length	3	Inch	
Width	3	Inch	
Height	1.5	inch	

Revision Number	History	Date
1.0	Document release	March 22, 2019

The information in this document is subject to change without notice and should not be construed as a commitment by Introspect Technology. While reasonable precautions have been taken, Introspect Technology assumes no responsibility for any errors that may appear in this document.