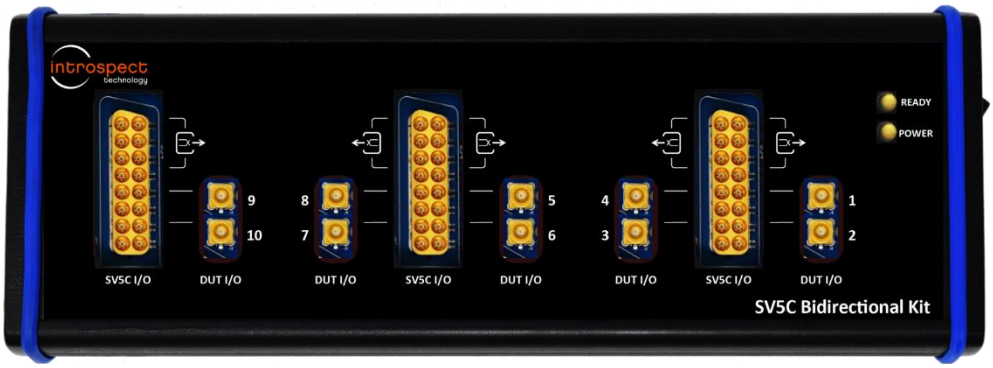
DATA SHEET

SV5C Bidirectional Kit

C SERIES



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Introduction

Introspect Technology's highly parallel SV5C pattern generator and signal analyzer is the ideal platform for DDR4 and DDR5 memory interface testing. The **SV5C Bidirectional Kit (BDK)** has been designed to integrate into any Introspect DDR test solution which requires bidirectional interface components. A single kit provides ten single-ended bidirectional lane capability with an analog bandwidth of 5 GHz. The figure below illustrates a typical connection of a SV5C Bidirectional Kit with an SV5C and a DDR device under test.

KEY FEATURES

- **Highly parallel:** ten bidirectional lanes, covering DQ and DQS DDR requirements
- **High performance:** 5 GHz analog bandwidth
- **Compact connection:** provides standard MXP cable connections to the Introspect SV5C and SMP connectors to DDR CTC2 test boards and similar test fixtures
- **Software controlled:** fully integrated into IESP software with existing DDR test suite offerings

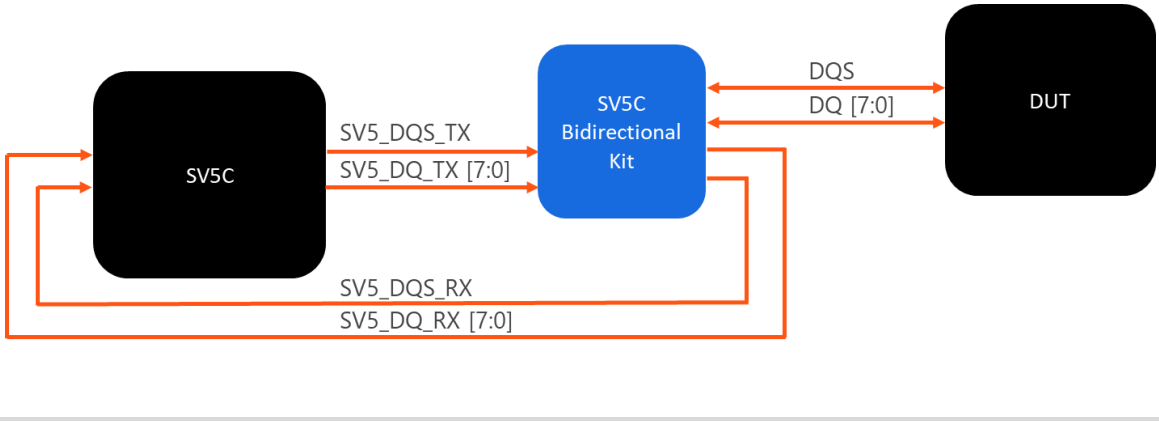


Figure 1: Example connection of the SV5C Bidirectional Kit in a DDR test application

PHYSICAL CONNECTIONS

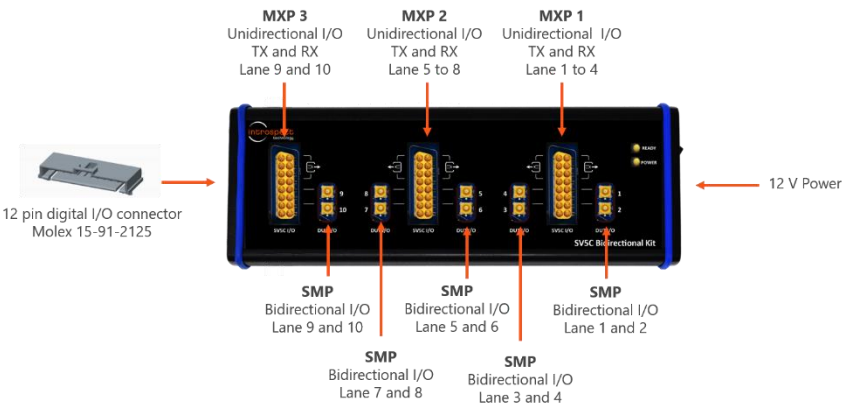
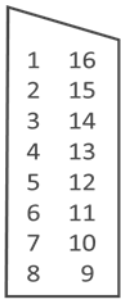


Figure 2: SV5C Bidirectional Kit physical connections

MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: MXP PINOUT ON THE SV5C BIDIRECTIONAL KIT

	MXP1 PIN	MXP1 SIGNAL	MXP2 PIN	MXP2 SIGNAL	MXP3 PIN	MXP3 SIGNAL
MXP Top View 	1	RX4P	1	RX8P	1	NC
	2	RX4N	2	RX8N	2	NC
	3	RX3P	3	RX7P	3	NC
	4	RX3N	4	RX7N	4	NC
	5	TX4P	5	TX8P	5	NC
	6	NC	6	NC	6	NC
	7	TX3P	7	TX7P	7	NC
	8	NC	8	NC	8	NC
	9	NC	9	NC	9	NC
	10	TX2P	10	TX6P	10	TX10P
	11	NC	11	NC	11	NC
	12	TX1P	12	TX5P	12	TX9P
	13	NC	13	RX6N	13	RX10N
	14	RX2P	14	RX6P	14	RX10P
	15	RX1N	15	RX5N	15	RX9N
	16	RX1P	16	RX5P	16	RX9

ORDERING INFORMATION

TABLE 2: ITEM NUMBERS FOR THE SV5C BIDIRECTIONAL KIT AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5780	SV5C Bidirectional Kit	Kit for enabling bidirectional DQ/DQS bus communications on SV5C
5712	SV5C-12 SerDes Tester	Per channel skew and jitter injection control, 12.5 Gbps maximum data rate
5713	SV5C-12 SerDes Tester (2 x 16 Channel Instruments)	Two-pack order code for receiving a complete 32-channel memory interface test solution. Consists of two 5712 instruments and associated calibration data
6604	SV4E-I3C - I3C Test and Debug Module	Three-in-one protocol exerciser, protocol analyzer, and device programmer for I3C and I3C-Basic devices

Features

BIDIRECTIONAL OPERATION

Figure 3 shows a high level diagram of the bidirectional lane in (a) SV5C transmit mode and (b) the SV5C in bus turnaround (BTA) mode / DUT transmit mode. The buffer shown in blue has a reference threshold voltage configurable in a range of 300 mV to 1200 mV. The 50 Ohm pull up when SV5C is in BTA mode originates from the SV5C Transmitter.

From the diagram below, note that the buffer shown in blue is always presenting a signal to the SV5C RX, whether its input signal is received from the SV5C TX as in Figure 3(a), or whether its input is the signal received from the DUT TX signal as in Figure 3(b). The following two figures provide examples of each.

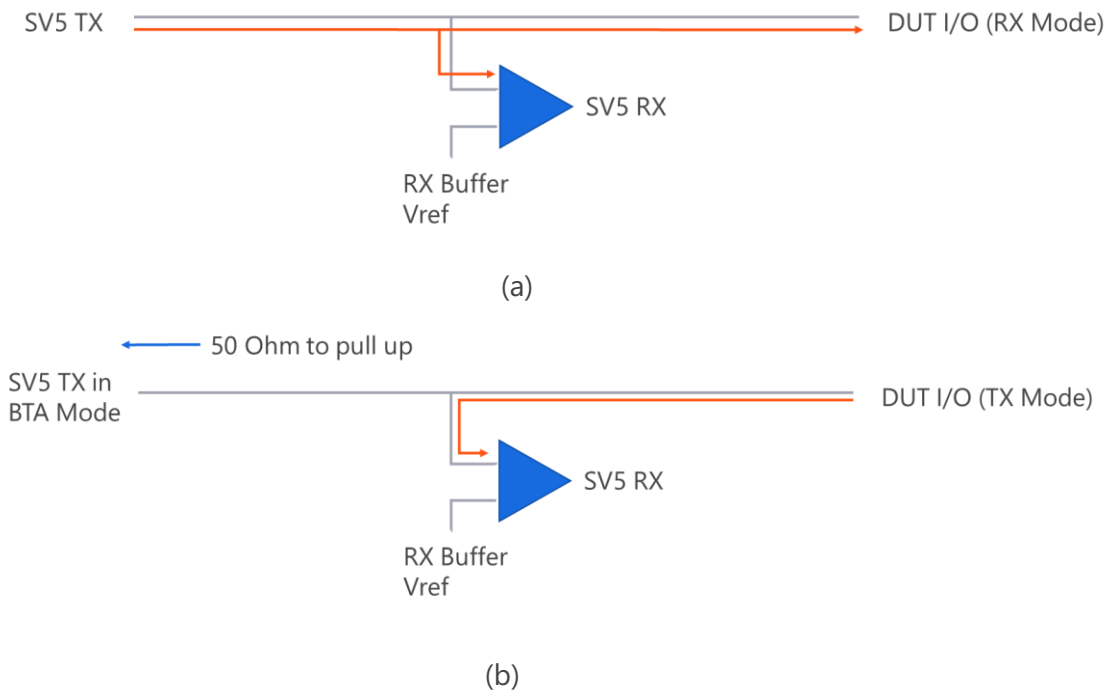


Figure 3: Bidirectional lane, (a) transmit and (b) receive signal directions

BIDIRETIONAL DATA CAPTURE

Figure 4 provides an example of the capabilities of SV5C and the Bidirectional Kit during a DDR memory write operation, when the SV5C is in transmit mode. The top left of the figure shows the signal path for this case, while the bottom left of the figure shows a timing diagram for the operation. The top right of the figure shows a capture of the DQS (blue) and one lane of DQ (purple) as displayed in the "Analog Data Capture" tool in the Introspect ESP Software, while the bottom right figure shows the capture as displayed in the "Digital Data Capture" tool in the Introspect ESP Software. All captures here were measured at a DDR data rate of 3.2 Gbps.

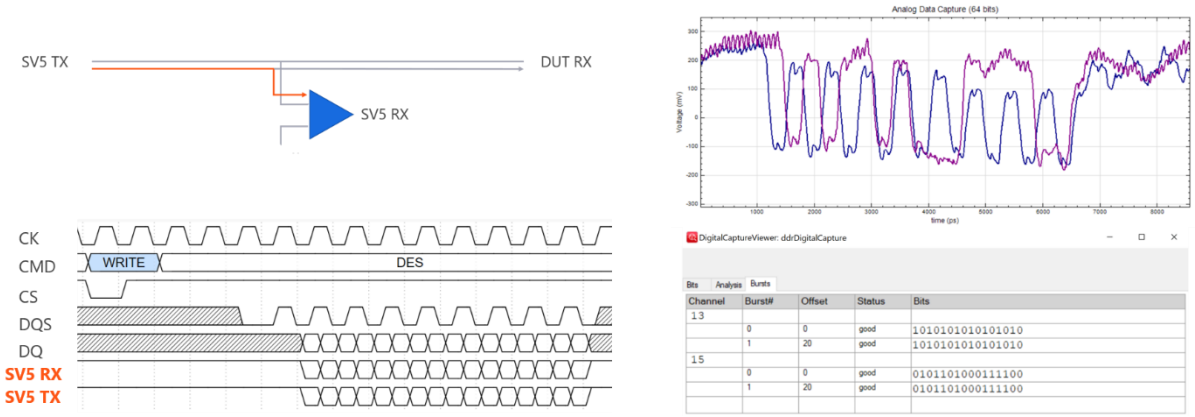


Figure 4: SV5C BDK Transmit Mode (DDR memory write operation)

A similar example is shown in Figure 5 for a DDR memory read, when the SV5C is in BTA mode / DUT transmit mode. The top left of the figure shows the signal path for this case, while the bottom left of the figure shows a timing diagram for the operation. The top right of the figure shows a capture of the DQS (blue) and one lane of DQ (purple) as displayed in the "Analog Data Capture" tool in the Introspect ESP Software, while the bottom right figure shows the capture as displayed in the "Digital Data Capture" tool in the software. Once again, all captures here were measured at a DDR data rate of 3.2 Gbps.

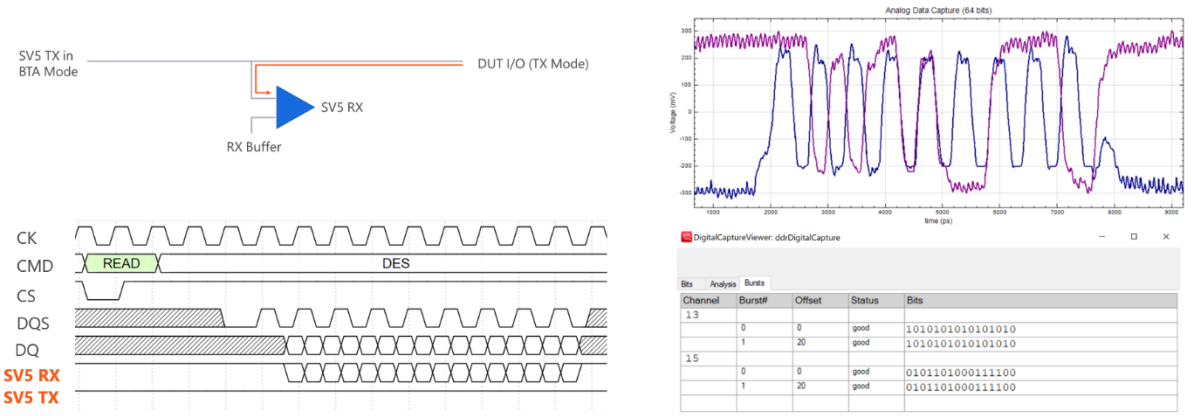


Figure 5: SV5C Bidirectional Kit BTA operation / DUT transmit mode (DDR memory read operation)

RX BUFFER REFERENCE VOLTAGE

Figure 6 demonstrates the effect of adjusting the input reference voltage on the RX buffer as viewed in the Introspect ESP Software "EyeScan" tool. The middle plot shows a capture of a DQ lane with the reference voltage set to the default reference voltage of 750 mV. The plots on the left and right show captures with the reference voltages set to 850 mV and 650 mV respectively. The full adjustment range for the reference is 300 mV to 1200 mV, allowing for optimal compensation and digital capture of single ended DDR signals.

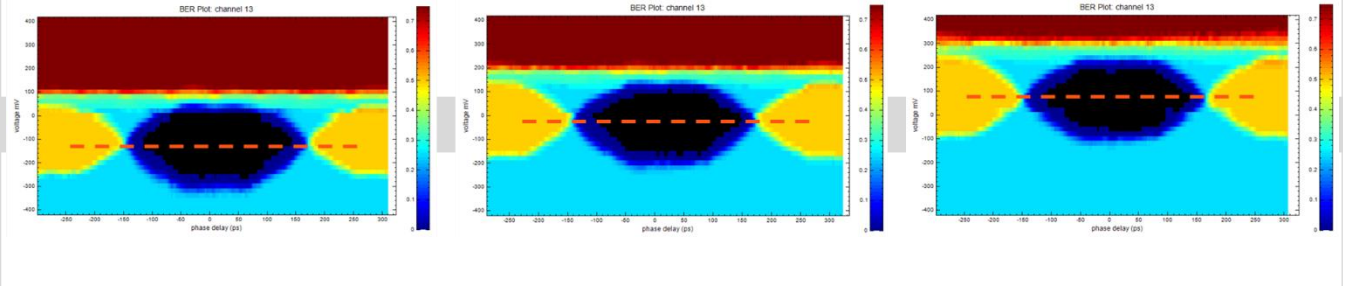


Figure 6: Adjustment of the RX buffer threshold level

Specifications

TABLE 3: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of Bidirectional Single Ended I/O lanes	10		Available via SMP connectors
Number of RX Voltage Buffers	10		One RX voltage buffer per lane
Power			
Voltage Supply	12	V	
Current Draw	TBD		
Data Rates and Timing			
Maximum Analog Bandwidth	5.0	GHz	
Maximum propagation delay SV5C transmit mode DUT transmit mode	 100 100	 ps ps	 MXP input to SMP output SMP input to MXP output
Receive Buffer Characteristics			
Minimum Input Threshold Voltage	300	mV	
Maximum Input Threshold Voltage	1200	mV	
Threshold Voltage Resolution	1	mV	
Buffer Load on bidirectional lane	> 1	kOhm	

Revision Number	History	Date
1.0	Document Release	October 22, 2020

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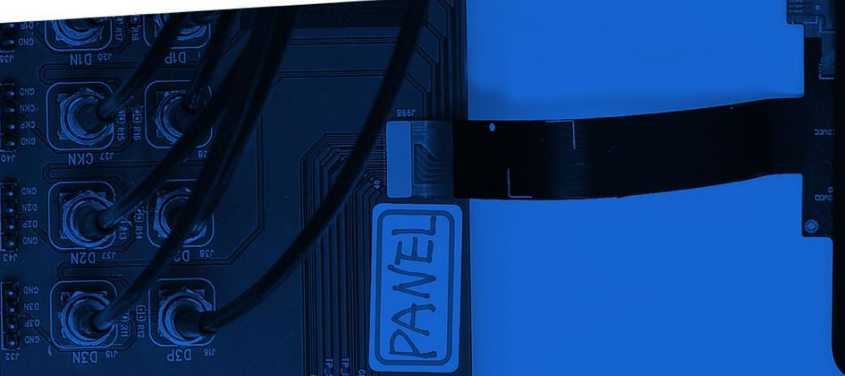

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