DATA SHEET

SV5C-DPRX

MIPI D-PHY Analyzer

C SERIES

Published in Canada on July 5, 2024
EN-D031E-E-24187

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Table of Contents

Introduction

OVERVIEW

The **SV5C-DPRX MIPI D-PHY Analyzer** is an ultra-portable, high-performance instrument that enables characterization and validation of MIPI D-PHY transmitter ports. The analyzer operates at up to 8.5 Gbps and combines analog signal measurement capabilities with sophisticated capture and compare modes for complete D-PHY packet analysis. The instrument operates using the highly versatile Pinetree software environment, including a full suite of tools for DSI-2 and CSI-2 video frame extraction. The software enables test automation for packet error rate testing, protocol timing analysis and MIPI CTS.

KEY FEATURES

- **D-PHY Physical Layer**: Four D-PHY lanes with integrated LP/HS signaling and support for a continuous range of data rates up to 8.5 Gbps.
- **D-PHY Protocol Layer:** Fully supports CSI-2 and DSI-2 pixel formats, DSI-2 DSC and V-DCM decompression, and DSI Display Command Sets (DCS).
- **Physical Layer Analysis**: Analog waveform capture for HS and LP with precision time stamps for physical layer events.
- **Protocol Layer Analysis**: Packet error rate testing, full video frame extraction and analysis, and sophisticated capture modes triggered on physical layer and protocol layer events.

KEY BENEFITS

- **Self-Contained**: An all-in-one system enables the simplest bench environment for physical layer test to full protocol layer validation.
- **Automated**: Leverages the full power of Python and the award-winning Pinetree software environment. Scripting capability is ideal for debug tasks and for full-fledged production screening of devices and systems.
- **Future Proof**: Protect your investment by adopting a high-performance tool for multiple product applications and across a large span of data rates.

PHYSICAL CONNECTIONS

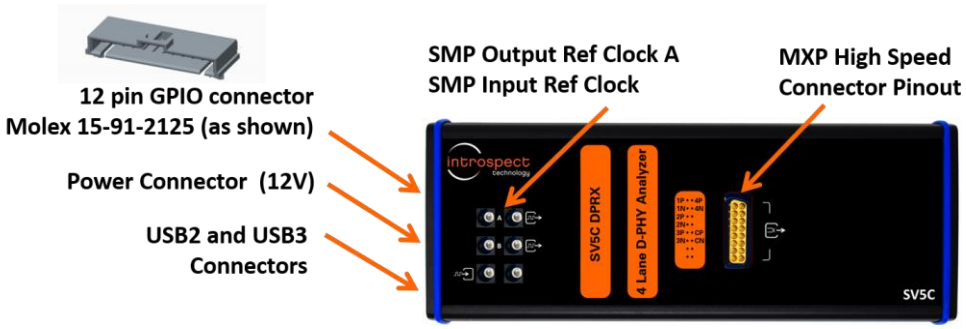
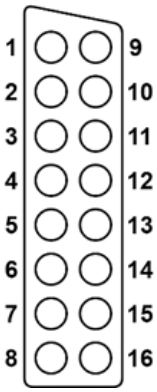


Figure 1: SV5C-DPRX physical connections.

MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: SIGNAL MAPPING OF THE MXP CONNECTOR FOR SV5C-DPRX

	MXP PIN	D-PHY PINOUT
MXP Top View  	1	Data Lane 1P
	2	Data Lane 1N
	3	Data Lane 2P
	4	Data Lane 2N
	5	Data Lane 3P
	6	Data Lane 3N
	7	NC
	8	NC
	9	Data Lane 4P
	10	Data Lane 4N
	11	NC
	12	NC
	13	Clock Lane P
	14	Clock Lane N
	15	NC
	16	NC

ORDERING INFORMATION

TABLE 2: ITEM NUMBERS FOR THE SV5C-DPRX AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5784	SV5C-DPRX MIPI D-PHY Analyzer (includes Pinetree SW license)	D-PHY physical and protocol layer analyzer for links up to 8.5 Gbps
5785	SV5C-CPRX MIPI C-PHY Analyzer (includes Pinetree SW license)	C-PHY physical and protocol layer analyzer for links up to 6.5 Gsps

Feature Description

COMPLETE D-PHY RECEIVER IMPLEMENTATION

The SV5C-DPRX MIPI D-PHY Analyzer is a complete, integrated, 4-lane D-PHY receiver providing the analog front-end circuitry for D-PHY as well as a complete protocol back-end. As shown in Figure 2, each lane contains low power (LP) programmable threshold voltage detectors, dynamically controlled termination resistors and fully differential high-speed (HS) receivers. The real-time behavior of the DPRX enables broad acquisition capabilities for physical-layer and protocol-layer testing. The analyzer also supports ALP-Mode operation.

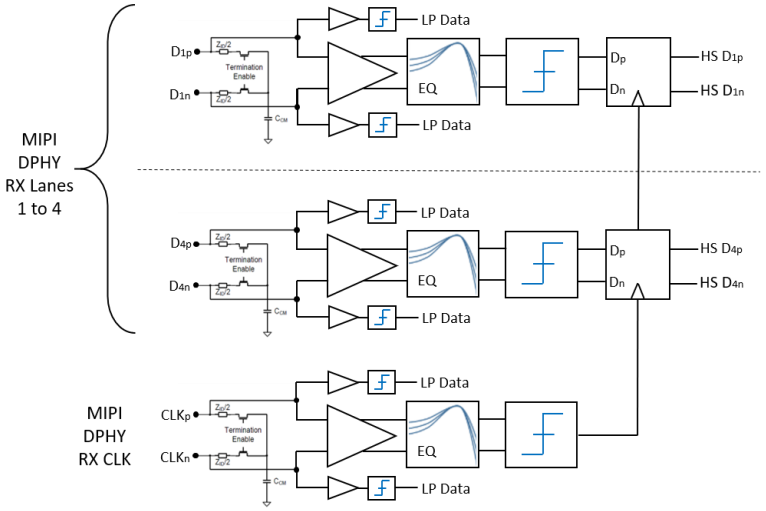
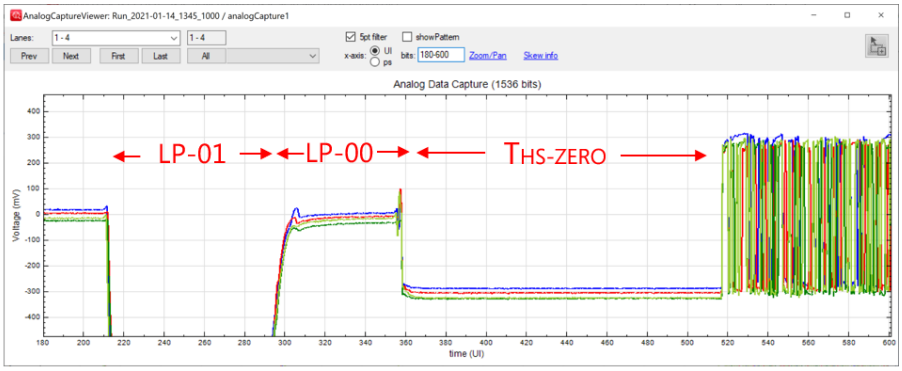


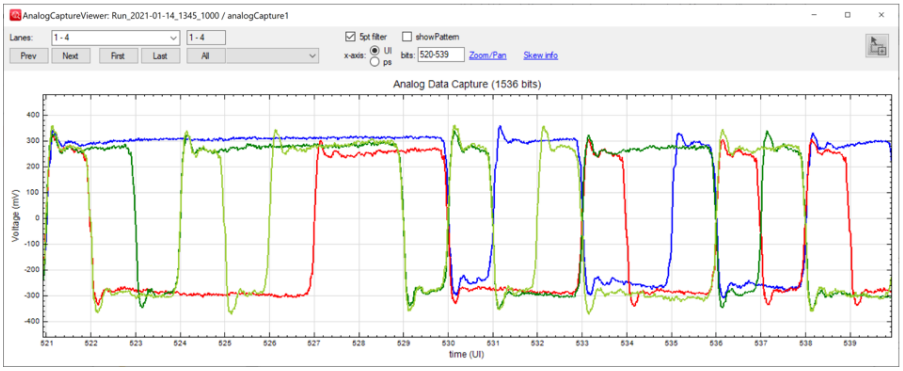
Figure 2: SV5C-DPRX receiver detail illustrating LP detection, automatic termination switches, and high-speed receivers.

ANALOG SIGNAL CAPTURE

The SV5C-DPRX provides analog waveform capture capability for both single ended LP and differential HS signals. Example captures are shown in Figure 3 below. Periodic HS signals can be sampled at a resolution of 128 points per UI for data rates up to 8.5 Gbps. HS measurements, including rise / fall time and voltage amplitude are automatically extracted. Periodic single-ended LP signals are sampled at a resolution of 2.5 ns. LP measurements including rise / fall time and amplitude are automatically extracted. High speed waveform acquisitions are triggered on packet starts, or may be triggered continuously, while LP signals may be triggered on several conditions including LP pulse width. The HS and LP analog capture tools enable deep-dive signal integrity investigations for physical layer debug and enable conformance testing such as the MIPI CTS.



(a)



(b)

Figure 3: SV5C-DPRX analog waveform capture capability in Pinetree: (a) LP and HS differential waveform, (b) close-up of differential HS waveform.

HARDWARE CRC CHECKING AND PACKET ERROR RATE TESTING

A fundamental feature of the SV5C-DPRX MIPI D-PHY Analyzer is hardware-based packet error-rate test (PERT) capability. Similar to the traditional BER test, the PERT enables the measurements of real D-PHY transmissions from CSI or DSI generators. As illustrated in Figure 4, the Analyzer detects and filters all signal waveforms and compares only the packet data transmitted between SOT and EOT, registering errors after the data has been merged between lanes, thereby comparing errors in packets rather than bits.

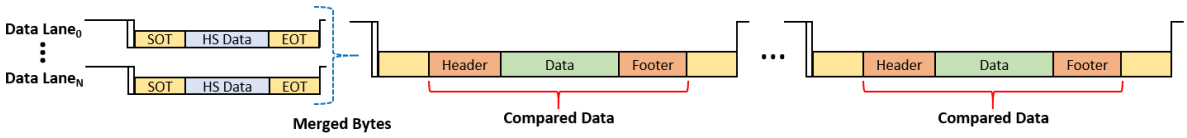


Figure 4: Illustration of packet error rate testing.

PROTOCOL ANALYSIS

The SV5C-DPRX MIPI D-PHY Analyzer is a complete protocol analyzer for both camera and display serial interfaces. The analyzer adjusts its viewer displays based on the protocol being measured. Figure 5 on the following page shows analysis features available in the Pinetree software, including viewers for:

- **HS Bursts:** View each high-speed burst with statistics of the time of arrival in nanoseconds, SOT offsets and byte-level data for each lane.
- **CSI/DSI Packets:** Merged traffic from all lanes may be viewed as unique packets, headers are decoded for easy, high-level viewing, and errors (header CRC, payload CRC, ECC) are automatically highlighted.
- **LP States**: Each LP state is captured along with its time of arrival and duration; this viewer is extremely effective for building a visualization of the physical layer events.
- **Frames**: Images are automatically reconstructed and saved, even if incomplete, with details such as pixel formats, data types, virtual channels, and image dimensions shown in the viewer.

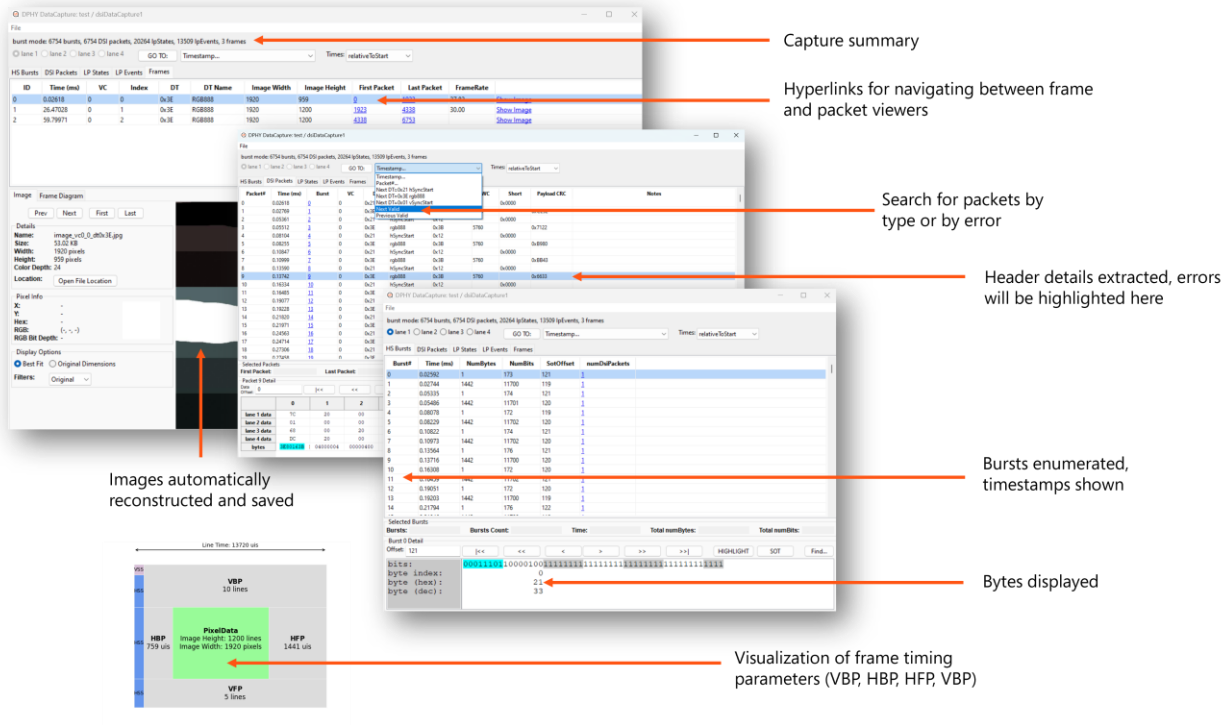


Figure 5: HS burst, packet, and frame viewers in Pinetree.

PROTOCOL ANALYSIS: ADVANCED TRIGGER MODES

Figure 6 shows the Pinetree user interface for defining the trigger mechanisms within the analyzer. At the highest level, the analyzer can be programmed to perform immediate captures (in which all data is measured irrespective of LP transitions) or as triggered captures. Each is as illustrated in Figure 5.

In triggered capture modes, the D-PHY analyzer automatically handles LP and HS received signals and resistor termination. The analyzer waits for a valid LP to HS entry sequence before enabling a capture, and when a valid HS-entry transition is detected, the capture starts immediately. If no valid HS-entry transition is detected, the capture returns an empty array.

Table 3 provides a list of trigger conditions that are available in the Analyzer. The duration of data captured before the trigger condition is specified in the software by “preTriggerDuration” settings. The duration of data captured after the trigger condition is specified in the software by “postTriggerDuration” settings. The specification of post trigger duration is described in the following section.

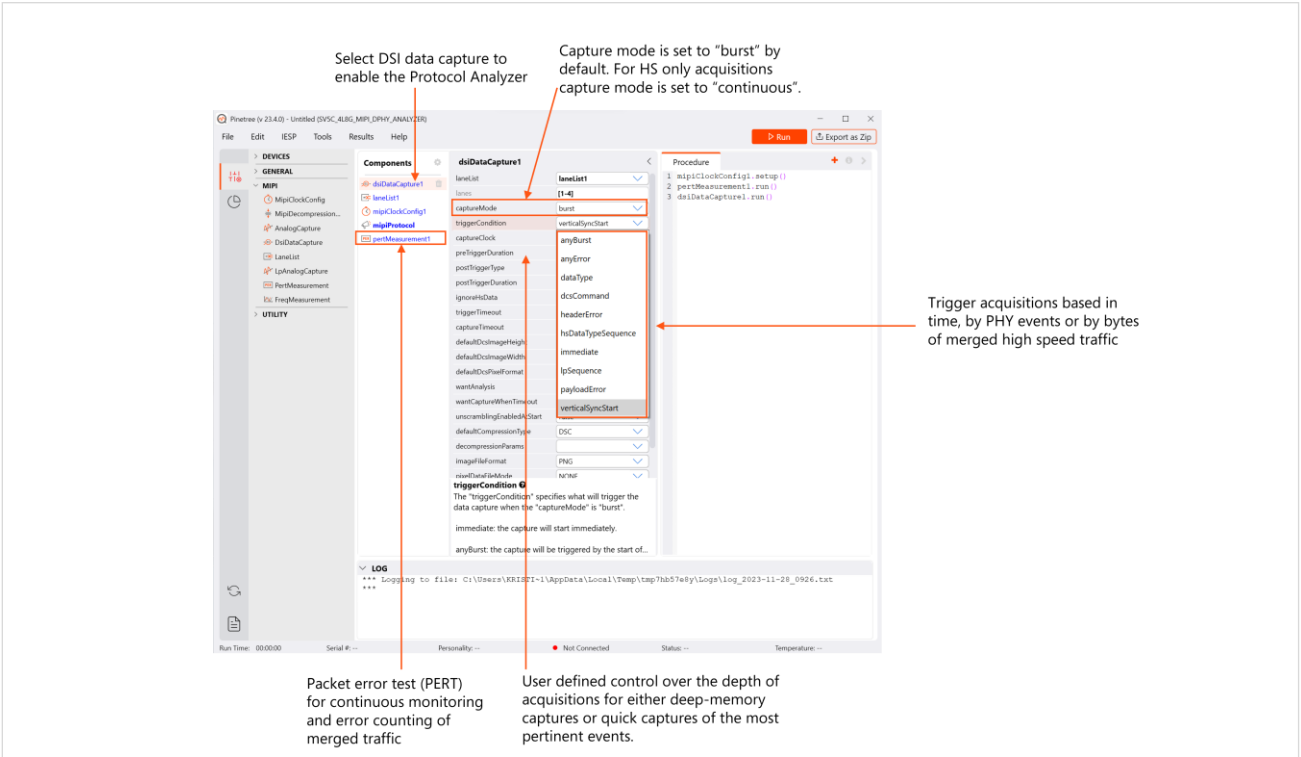


Figure 6: Example of Pinetree GUI test setup and trigger mechanisms for the SV5C-DPRX. Top left: Components window, showing selected CSI, DSI and PHY data acquisition methods. Center: Properties window, showing DSI Data Capture. Bottom: Log (Test Procedure) window, with Python code calling components.

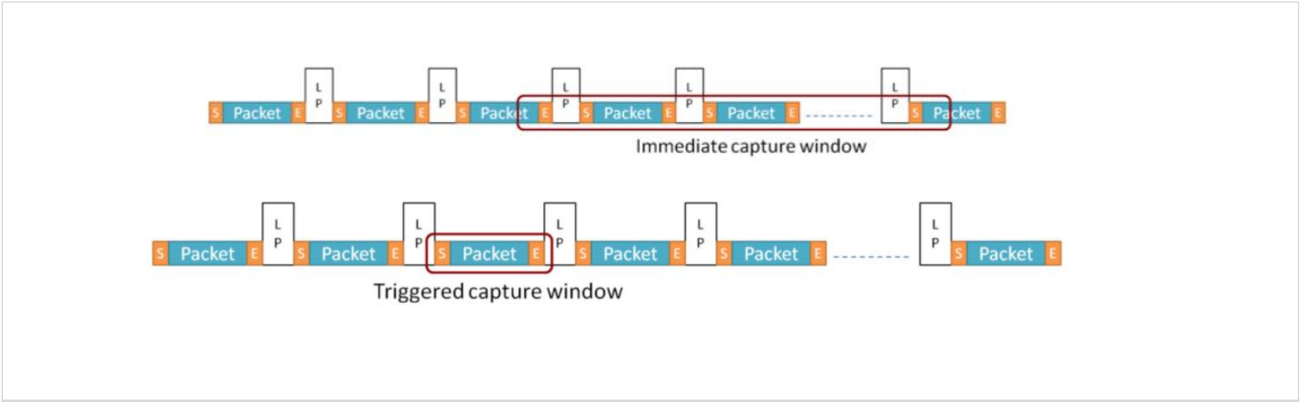


Figure 7: Illustration of multi-packet, per lane PHY-level capture (top) and triggered packet capture (bottom).

TABLE 3: TRIGGER CONDITIONS

TRIGGER CONDITION NAME	TYPE OF EVENT	TRIGGER DESCRIPTION
Immediate	Time-Based	time-based acquisition, beginning immediately
anyBurst	PHY	the first high-speed burst recorded on any data lane
lpSequence	PHY	user-defined sequence of LP states, e.g. "11,01,00" reflects a proper LP-HS entry sequence
anyError	CSI, DSI	the first error is registered: header, CRC, or payload
dataTypeSequence	CSI, DSI	user-defined integer value to be identified in a packet header
headerError	CSI, DSI	protocol layer, the first error recognized in a packet header
payloadError	CSI, DSI	protocol layer, the first error recognized in a packet header
firstPayloadByte	CSI, DSI	user-defined byte to be identified in the payload
lpPacketDataType	CSI, DSI	user-defined integer value to identified in LP packet
frameStart	CSI	CSI-only, any packet with header data type 0x00 indicating the beginning of a frame
verticalSyncStart	DSI	DSI-only, any packet with header data type 0x01 indicating the beginning of a frame

PROTOCOL ANALYSIS: ACQUISITION DURATION

The acquisition duration is determined according to the "postTriggerType", and it may be specified in terms of time, in terms of PHY events, or in terms of bytes of merged high-speed traffic. Figure 8 illustrates two methods of determining acquisition length in terms of PHY events. In Figure 8 (top), an acquisition begins on the first high-speed burst observed and completes after a user-defined number of bursts are recorded. In Figure 8 (bottom), an acquisition begins and the analyzer records for a user-defined period of N nanoseconds.

On the next page, Figure 9 illustrates three examples of triggering acquisitions on merged, high-speed data. The acquisition start condition is user-defined as either: (a) an error within a packet header, (b) a variable data type identifier, here chosen as 0x01 or (c) a frame start packet (CSI only). The duration of the acquisition for each is chosen according to the number of N received: (d) bursts, (e) bytes or (f) frame end packets.

Table 4 provides a list of conditions for determining the acquisition duration.

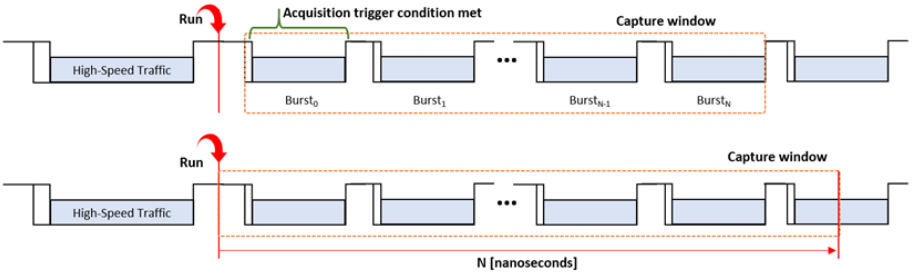


Figure 8: Illustration of two event-based acquisitions. Above, acquisition is triggered on the first observed burst and the duration is determined by a user-defined number of N bursts. Below, acquisition begins immediately, and the duration is for a user-defined period of N nanoseconds.

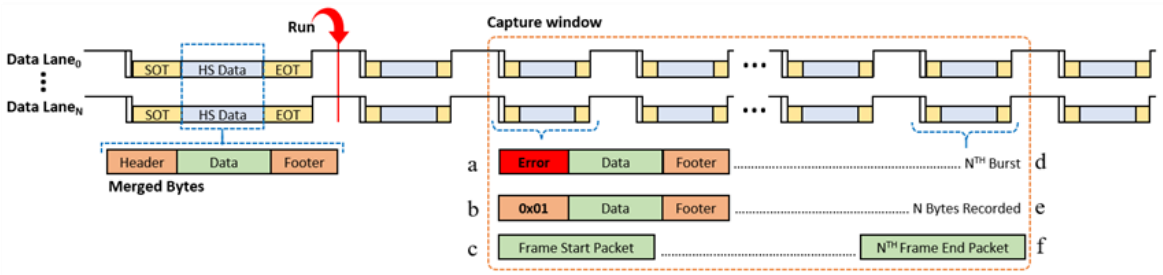


Figure 9: Illustration of three acquisitions triggered on merged high-speed traffic events: (a) a header error, (b) a user-defined data type identifier and (c) a frame start packet. Three conditions for specifying the acquisition duration are shown: (d) a user-defined number of N bursts, (e) a number of bytes, and (f) a number of frames.

TABLE 4: SPECIFICATION OF ACQUISITION DURATION

SPECIFICATION OF ACQUISITION DURATION	TYPE OF EVENT	TRIGGER DESCRIPTION
durationInNs	Time-Based	time-based acquisition, defined in nanoseconds
numberOfBursts	PHY	the total number of unique bursts acquired, across all data lanes
numberOfBytes	PHY	the total number of bytes recorded between SOT and EOT of all bursts
numberOfLpCommands	PHY	the number of LP commands acquired
numberOfLpStates	PHY	The number of unique LP states, e.g. “11,01,00” would be 3 states
numberOfFrameEnds	CSI	protocol layer, the number of frame-end packets recorded
numberOfVerticalSyncStarts	DSI	protocol layer, the number of packets with data type identifier 0x01

Specifications

TABLE 5: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	D-PHY		
MIPI Protocol	CSI, DSI		CSI-2 v1.3, v2.0, v3.0, DSI-2 v1.1
LS/HS Handling	Automatic		
ALP Mode	Yes		
Ports			
Number of D-PHY Lanes	4 Lanes and CLK		Supports embedded clock for MIPI D-PHY v3.5
Number of Dedicated Low-Speed Output Reference Clocks	2		Individually synthesized frequency and output format
Number of Dedicated Input Reference Clocks	1		Used as external reference clock input
Number of Trigger Inputs	2		Via Molex connector
Number of Flag Outputs	2		Via Molex connector
Number of I2C/I3C Masters	1		Two pins: SCL and SDA via Molex connector
Connections to PC for Pinetree Control	2		USB2 (module control) USB3 (data transfer)
Power Consumption			
DC Input Voltage	12	V	
Maximum Current Draw	TBD	A	

TABLE 6: D-PHY DATA RATES AND REFERENCE CLOCKS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Data Rates / Frame Rates			
Minimum HS Data Rate	80	Mbps	Per Lane
Maximum HS Data Rate	8.5	Gbps	Per Lane
Frequency Resolution of HS Data Rate	1	kbps	
Minimum LP Toggle Rate	0	MHz	
Maximum LP Toggle Rate	20	MHz	
Reference Clock Frequencies			
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	500	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Output Clock I/O Standards			LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 7: D-PHY RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Impedance	50	ohm	HS transmission, each wire
Input Impedance	Hi-Z		LP transmission
HS / LP Voltage			
Minimum $\|V_{ID}\|$	90	mV	At SV5C MXP connector
Maximum $\|V_{ID}\|$	600	mV	At SV5C MXP connector
Minimum Programmable LP Threshold	-100	mV	
Maximum Programmable LP Threshold	1300	mV	
Timing Generator Performance			
Timing Resolution	7.8125	mUI	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		
Global Timing Performance			
Minimum T_{LPX}	50 ns		
Minimum $T_{HS\text{-}PREPARE}$	40 ns + 4 UI		
Minimum $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	145 ns + 10 UI		
Minimum $T_{HS\text{-}TRAIL}$	Larger of: (60 ns + 4 UI) or 8 UI		
Minimum $T_{CLK\text{-}PREPARE}$	38 ns		
Minimum $T_{CLK\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	300 ns		
Minimum $T_{CLK\text{-}PRE}$	8 UI		
Minimum $T_{CLK\text{-}POST}$	60 ns + 52 UI		
Minimum $T_{CLK\text{-}TRAIL}$	60 ns		

TABLE 8: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Supported Pixel Formats (CSI)	RAW, RGB, YUV		RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, RGB444, RGB555, RGB565, RGB666, RGB888, YUV420, YUV422
Supported Pixel Formats (DSI)	RGB YCbCr		RGB101010, RGB121212, RGB332, RGB565, RGB666, RGB888, YCbCr420_12bit, YCbCr422_16bit, YCbCr422_20bit, YCbCr422_24bit
Decompression Support (DSI)	Yes		DSC, V-DCM
Display Command Set (DSI) Support	Yes		
Memory Depth	8	GByte	For received packet data

TABLE 9: PACKET AND FRAME ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
HS Data Rate Detection	Yes		Automatic
CSI / DSI Packet Analysis	Yes		Header, Payload, ECC extraction, data type detection, virtual channel support
Frame Analysis	Yes		Image width / height detection Pixel format and frame rate detection
CRC and ECC Analysis	Yes		Payload error and header error detection, Packet error statistics
Trigger Conditions for Data Capture	Yes		Refer to Table
Specification of Data Acquisition Duration	Yes		Refer to Table

TABLE 10: TRIGGER, FLAG, AND I2C BUS VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	1.8	V	All GPIOs operate at 1.8 V LVCMOS
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.6	V	
V_{IH} minimum	1.2	V	
V_{IH} maximum	2.1	V	
V_{OL} maximum	0.45	V	
V_{OH} minimum	1.35	V	

REVISION NUMBER	HISTORY	DATE
1.0	Document Release	January 15, 2021
1.1	Updated Figures 5 and 6, and software mentions to Pinetree	November 28, 2023
1.2	Added support for embedded clock in Table 5	July 5, 2024

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Published in Canada on July 5, 2024
EN-D031E-E-24187

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