REFERENCE DESIGN GUIDE

SV4E-DPRX

Device Adapter Board (DAB)

E SERIES

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Introduction

OVERVIEW

The SV4E-DPRX Analyzer and SV4E-DPRXG Frame Grabber are highly integrated instruments designed for testing MIPI® Alliance D-PHY enabled devices. A device adapter board (DAB) forms the physical interface between an SV4E-DPRX / SV4E-DPRXG and a customer device under test (DUT). The DAB provides the connections for all high-speed D-PHY signals, low speed GPIO signal pins, and any power supply pins for the DUT, if required. This document provides the information required for customers to design the DAB for their specific test application.

A reference design (schematic, layout, and bill of materials) for an example DAB is available. Please contact Introspect Technology for access to this reference design.

Device Adapter Board (DAB) Ports and Connectors

PHYSICAL CONNECTIONS

Figure 1(a) and (b) show the ports and connectors on the SV4E-DPRX. The connection of a typical DAB is shown in Figure 1(c). The DAB provides the physical interface between the SV4E-DPRX to the DUT (in this case, a sensor under test).

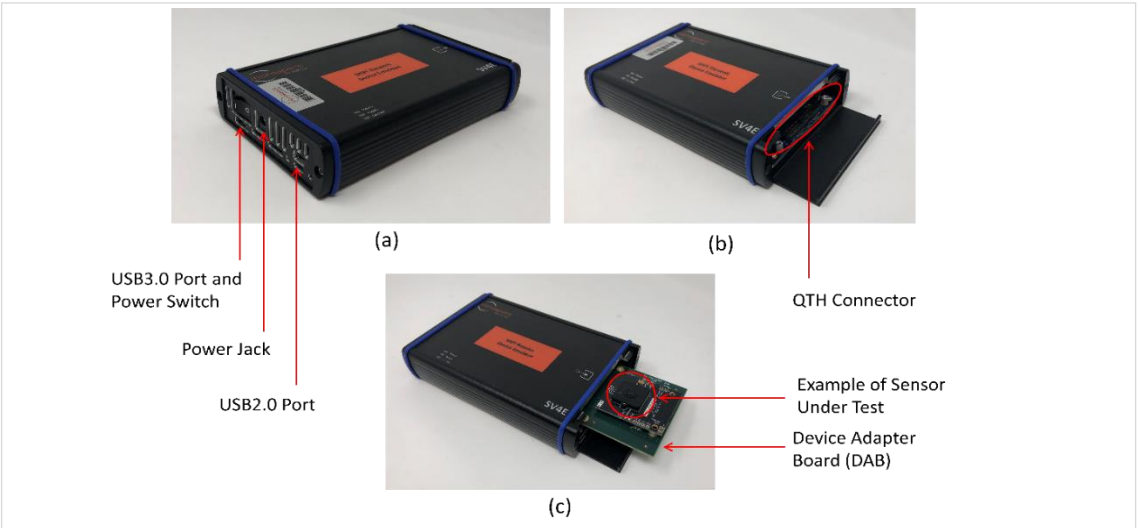


Figure 1: SV4E-DPRX connectors: (a) left side (b) right side (c) typical DAB connection

A diagram outlining the mechanical connection of a DAB to SV4E-DPRX is shown in **Error! Reference source not found.** below. The stiffener, spacers, and screws are included as standard parts of the SV4E-DPRX construction.

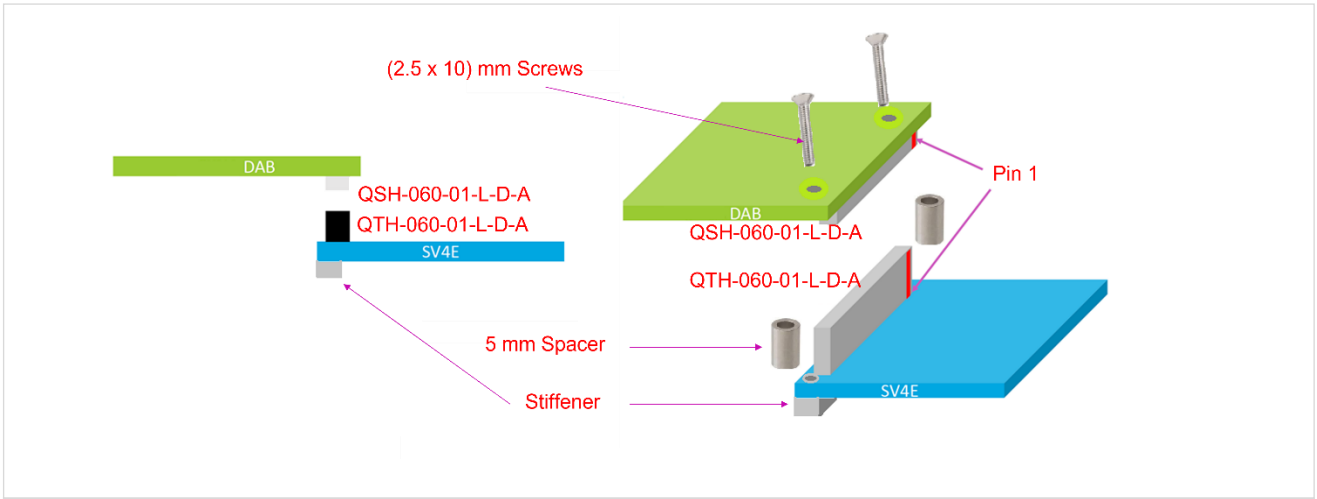


Figure 2: Mechanical connection between the SV4E-DPRX circuit board and DAB

REFERENCE DESIGN: DEVICE ADAPTER BOARD (DAB)

A reference design for a DAB is available from Introspect Technology. Photographs of the top and bottom of the reference design are shown in Figure 3.

The reference design shown in Figure 3 provides the required QSH connector (J57) for attachment to the SV4E-DPRX. Direct access to high-speed D-PHY signals is provided via SMA connectors (J9 to J18). Access to several GPIO pins is provided via a right-angle 0.1" header (J20 in the figure). This DAB has been designed as a generic interface and may be used as a prototype for any DUT.

The following sections provide additional connection details which may be required by a customer DAB.

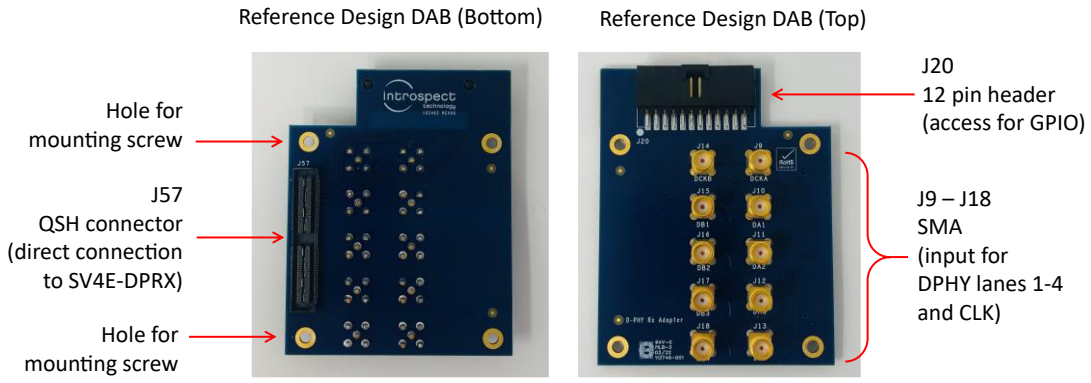


Figure 3: Photogram of the reference design for the DAB. Top and bottom of the DAB are shown.

QTH / QSH CONNECTORS

The SV4E-DPRX has a 120 pin, high-speed connector for all inputs and outputs, with part number Samtec QTH-060-01-L-D-A. This part is designed to mate to a high-speed connector on the customer adapter board using the following part number:

Part Number: Samtec QSH-060-01-L-D-A

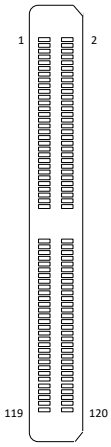
https://www.samtec.com/products/qsh

All signals between the SV4E-DPRX and the DAB connect through this single QTH / QSH connector combination.

QSH HIGH SPEED SIGNAL CONNECTIONS

The pinout for the high-speed D-PHY signals on the QSH connector is given in Table 1. The ground pins specified below should be implemented on the DAB even if not all lanes are used in a particular application.

TABLE 1: SV4E DAB HIGH SPEED SIGNAL PINS

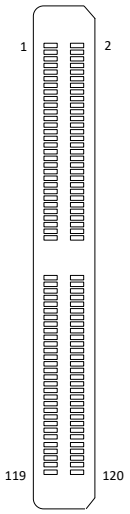
FOOTPRINT	QSH PIN NUMBER	SV4E-DPRX REFERENCE DAB SCHEMATIC NAME	PIN DESCRIPTION
QSH-060-01-L-D-A (QSH top view, placed on bottom side of DAB) 	37	D_BUS_A_CK	D-PHY RX CLKP
	39	D_BUS_B_CK	D-PHY RX CLKN
	43	D_BUS_A1	D-PHY RX Data Lane 1P
	45	D_BUS_B1	D-PHY RX Data Lane 1N
	49	D_BUS_A2	D-PHY RX Data Lane 2P
	51	D_BUS_B2	D-PHY RX Data Lane 2N
	55	D_BUS_A3	D-PHY RX Data Lane 3P
	57	D_BUS_B3	D-PHY RX Data Lane 3N
	61	D_BUS_A4	D-PHY RX Data Lane 4P
	63	D_BUS_B4	D-PHY RX Data Lane 4N
	35, 41, 47, 53, 59, 65	Ground	Required ground connections

QSH GPIO CONNECTIONS

The pinout for the general purpose I/Os (GPIOs) on the QSH connector is given in Table 2. The names and functions are fixed for the first five GPIO pins. Other GPIO pins (GPIO_A5 to GPIO_A15, as labelled in the DAB schematic) may be used to implement other functions directly in IESP software. Please consult with Introspect if other GPIOs are intended for customer use.

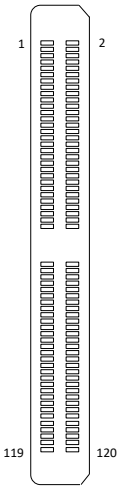
All pins below are compatible with LVCMOS 1.8 V logic.

TABLE 2: SV4E DAB GPIO PINS

FOOTPRINT	QSH PIN	SV4E-DPRX REFERENCE DAB SCHEMATIC NAME	IESP SOFTWARE NAME	I/O	DESCRIPTION
QSH-060-01-L-D-A (QSH top view, placed on bottom side of DAB) 	2	GPIO_A0	RESET_N	I	SV4E reset pin, active low ("0" = reset, "1" = not in reset)
	4	GPIO_A1	USER I3C SCL	O	General purpose I2C / I3C bus (SV4E is master)
	8	GPIO_A2	USER I3C SDA	I/O	General purpose I2C / I3C bus (SV4E is master)
	10	GPIO_A3	FRAME_START/ END	O	Asserted to "1" on frame start, Deasserted to "0" on frame end
	14	GPIO_A4	LINE_START/ END	O	Asserted to "1" on line start, Deasserted to "0" on line end
	16	GPIO_A5	GPIO[1]	I/O	User configurable (Input/Output)
	20	GPIO_A6	GPIO[2]	I/O	User configurable (Input/Output)
	22	GPIO_A7	GPIO[3]	I/O	User configurable (Input/Output)
	26	GPIO_A8	GPIO[4]	I/O	User configurable (Input/Output)
	28	GPIO_A9	GPIO[5]	I/O	User configurable (Input/Output)
	32	GPIO_A10	GPIO[6]	I/O	User configurable (Input/Output)
	34	GPIO_A11	GPIO[7]	I/O	User configurable (Input/Output)
	38	GPIO_A12	GPIO[8]	I/O	User configurable (Input/Output)
	40	GPIO_A13	GPIO[9]	I/O	User configurable (Input/Output)
	44	GPIO_A14	GPIO[10]	I/O	User configurable (Input/Output)
	46	GPIO_A15	GPIO[11]	I/O	User configurable (Input/Output)
	6, 12, 18, 24, 30, 36, 42, 48	Ground	-	-	Required ground connections

For the purposes of prototyping, the reference DAB (as pictured in Figure 3) provides easy access to several of the GPIO pins via the J20 connector. Please refer to Table 3 below for the direct mapping between the J57 QSH pins, the J20 header pins, and the IESP software naming conventions for the programmable GPIOs.

TABLE 3: GPIO PINS SUPPORTED BY THE REFERENCE DESIGN DAB

FOOTPRINT	QSH PIN	SV4E-DPRX REFERENCE DAB PIN ON J20	IESP SOFTWARE NAME	I/O	DESCRIPTION
QSH-060-01-L-D-A (QSH top view, placed on bottom side of DAB) 	2	10	RESET_N	I	SV4E reset pin, active low ("0" = reset, "1" = not in reset)
	4	9	USER I3C SCL	O	General purpose I2C / I3C bus (SV4E is master)
	8	8	USER I3C SDA	I/O	General purpose I2C / I3C bus (SV4E is master)
	10	7	FRAME_START/ FRAME END	O	Asserted to "1" on frame start, Deasserted to "0" on frame end
	14	6	LINE_START/ LINE END	O	Asserted to "1" on line start, Deasserted to "0" on line end
	16	5	GPIO[1]	I/O	User configurable (Input/Output)
	20	4	GPIO[2]	I/O	User configurable (Input/Output)
	22	3	GPIO[3]	I/O	User configurable (Input/Output)
	26	2	GPIO[4]	I/O	User configurable (Input/Output)
	28	1	GPIO[5]	I/O	User configurable (Input/Output)
	32	*	GPIO[6]	I/O	User configurable (Input/Output)
	34	*	GPIO[7]	I/O	User configurable (Input/Output)
	38	*	GPIO[8]	I/O	User configurable (Input/Output)
	40	*	GPIO[9]	I/O	User configurable (Input/Output)
	44	*	GPIO[10]	I/O	User configurable (Input/Output)
	46	*	GPIO[11]	I/O	User configurable (Input/Output)
	6, 12, 18, 24, 30, 36, 42, 48	-	-	-	Ground connections
	-	12	-	I/O	Ground connection

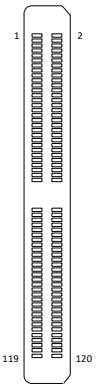
* Not routed on the reference schematic, but available on the SV4E.

QSH PROGRAMMABLE POWER SUPPLIES

The QSH connector provides access to six programmable power supplies which may be used on the DAB. The programmable range of these supplies is between 1.0 V to 5.0 V, in steps of 1 mV, with a maximum supply current of 3.0 A for each supply.

The pinout for these supplies is specified in Table 4. If used, please ensure that appropriate decoupling is applied (100 nF minimum per supply).

TABLE 4: SV4E DAB, PROGRAMMABLE POWER SUPPLIES

FOOTPRINT	QSH PIN NUMBER	NAME	DESCRIPTION
QSH-060-01-L-D-A (QSH top view, placed on bottom side of DAB 	50	PV1_OUT	Programmable Power Supply # 1 Output Pin
	52	PV1_OUT	Programmable Power Supply # 1 Output Pin
	56	PV2_OUT	Programmable Power Supply # 2 Output Pin
	58	PV2_OUT	Programmable Power Supply # 2 Output Pin
	62	PV3_OUT	Programmable Power Supply # 3 Output Pin
	64	PV3_OUT	Programmable Power Supply # 3 Output Pin
	67	PV4_OUT	Programmable Power Supply # 4 Output Pin
	69	PV4_OUT	Programmable Power Supply # 4 Output Pin
	109	PV5_OUT	Programmable Power Supply # 5 Output Pin
	111	PV5_OUT	Programmable Power Supply # 5 Output Pin
	115	PV6_OUT	Programmable Power Supply # 6 Output Pin
	117	PV6_OUT	Programmable Power Supply # 6 Output Pin
	48, 54, 60, 65, 66, 71, 107, 113, 119	Ground	Required ground connections

Additional Documentation

SV4E-DPRX Analyzer Datasheet

- EN-D020E-E-22167 SV4E DPRX D-PHY Analyzer Data Sheet

SV4E-DPRX Frame Grabber Datasheet

- EN-D022E-E-22171 SV4E DPRXG D-PHY Frame Grabber Data Sheet

SV4E-DPRX DAB Design Files.zip

- Includes reference schematic (.pdf), layout files (.brd), and Bill of Materials (.xlsx) for the example DAB. Please contact Introspect Technology for access to the reference design.

Revision Number	History	Date
1.0	Document release	March 25, 2020
1.1	Updated pinout for QSH-060 connector and updated signal names for the new reference adapter board and design files.	May 13, 2022
1.2	Minor changes to QSH-060 connector description and to the “Additional Documentation” section.	August 5, 2022

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