USER GUIDE

# DDR5 DRAM Test Suite Calibration Scripts

## C SERIES



Published in Canada on April 23, 2021
EN-G056E-E-21113

INTROSPECT.CA

# Table of Contents

# Introduction

This document outlines the calibrations that must be performed prior to using the DDR5 DRAM Test Suite. There are two calibrations, one to measure the command to data skew and one to measure the data bus latency through the test bench. The two calibrations differ only in the test bench setup, the same test procedure is used for both.

# Test Bench Setup

Refer to the document "EN-G057E-E-21113 DDR5 DRAM Test Suite User Guide" for information on setting up the test bench and connecting the SV5C 32 channel bidirectional system.

Figure 1 shows the labelling of each cable assembly, which will be referenced in the sections below. The cable types denoted in Figure 1 refer to the endpoints only, there may be additional cables that make up the assembly. For example, cable 3 is labeled as MXP-MXP, but may consist of 2 MXP-SMA cables. Unless specified otherwise, it is important to calibrate with the exact cable assemblies that will be part of the final test bench.

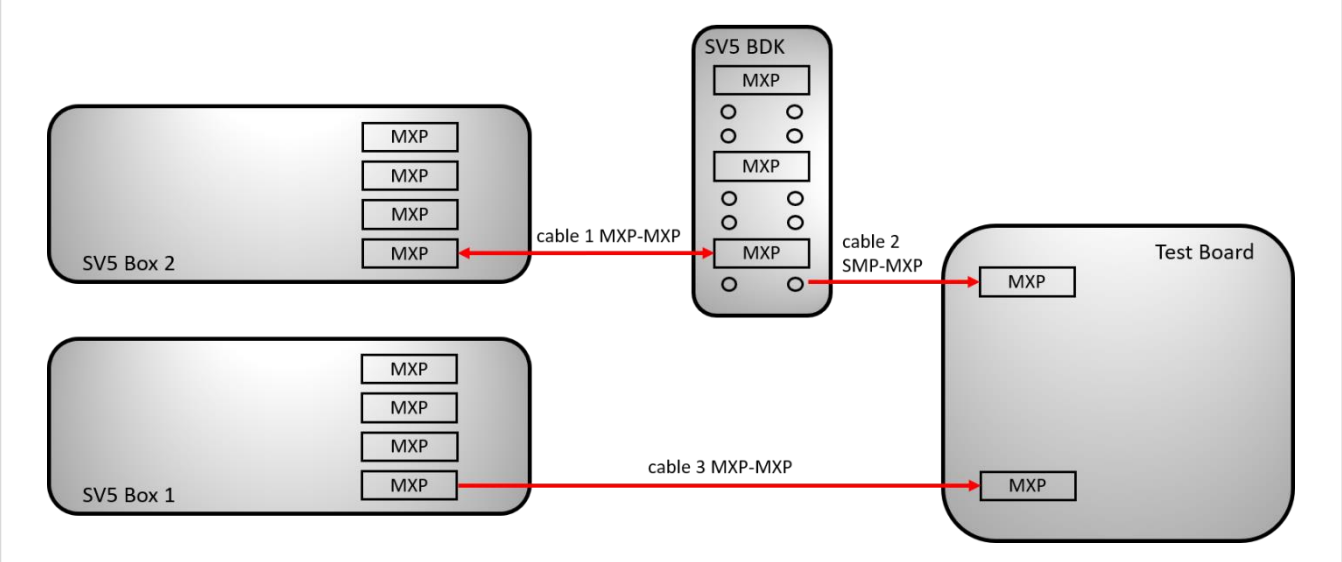


**Figure 1**: SV5C DDR5 Test Bench Connections

## COMMAND TO DATA SKEW CALIBRATION

The purpose of this calibration is to measure the skew difference between the command address bus path through cable 3, and the data bus path through cable 1, the SV5C bidirectional kit and cable 2. Figure 2 shows the connections required for this calibration. Table 1 provides the channel numbers for these connections.

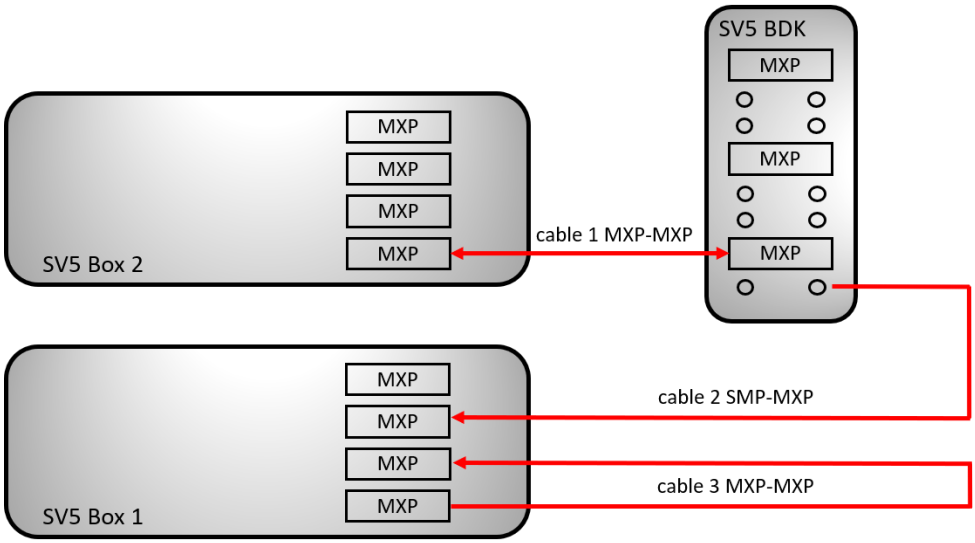


**Figure 2**: Connections for the Command to Data Skew Calibration

## DATA BUS LATENCY CALIBRATION

Figure 3 shows the connections required for the data bus latency calibration. Table 1 provides the channel numbers for these connections. The MXP-MXP connection denoted cable x does not need to be the same as cable 1 or cable 3 in Figure 1, but the same cable assembly must be used for both connections required in the calibration.

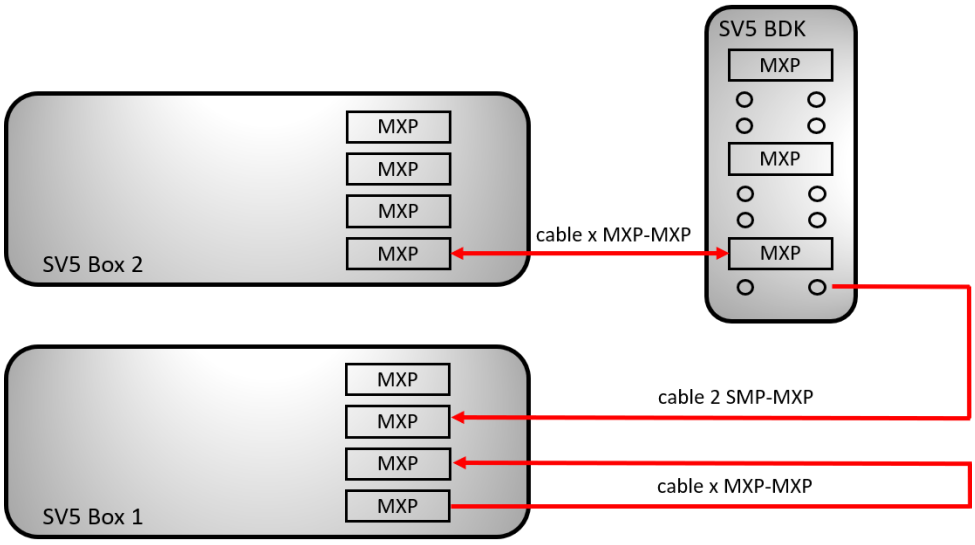


**Figure 3**: Connections for the Data Bus Latency Calibration

## TABLE 1: DDR5 DRAM CALIBRATION CONNECTIONS

| TX CONNECTIONS | RX CONNECTIONS |
|---|---|
| SV5C TX1P | SV5C RX5P |
| SV5C TX1N | SV5C RX5N |
| SV5C TX17P | BDK TX1P |
| SV5C TX17N | BDK TX1N |
| BDK RX1P | SV5C RX17P |
| BDK RX1N | SV5C RX17N |
| BDK DUT 1 | SV5C RX9P |
| DC block and 50 Ohm term | SV5C RX9N |

# Running the Calibration

The same test procedure is used for both calibrations. Open the test procedure folder "DRAMTestSuiteCal" in the Introspect ESP Software GUI with the SV5C_32C12G_BIDIR_DDR form factor and follow the steps below.

1. Setup the test bench for the command to data skew calibration.
2. Click 'run' to start the execution of the calibration.
3. The calibration will generate a file "calOutput.txt" in the Params folder of the test procedure. Rename this file to "commandToDataSkewCal.txt".
4. Repeat steps 1-3 for the data bus latency calibration, renaming the output file to "dataBusLatencyCal.csv".
5. Open the DDR5 DRAM Test Suite procedure and enter the value from "commandToDataSkewCal.txt" for *dramController.calibratedCommandToDataSkew*, and the value from "dataToCommandSkewCal.txt" for *dramController.calibratedDataBusLatency*. See Figure 4 as an example.

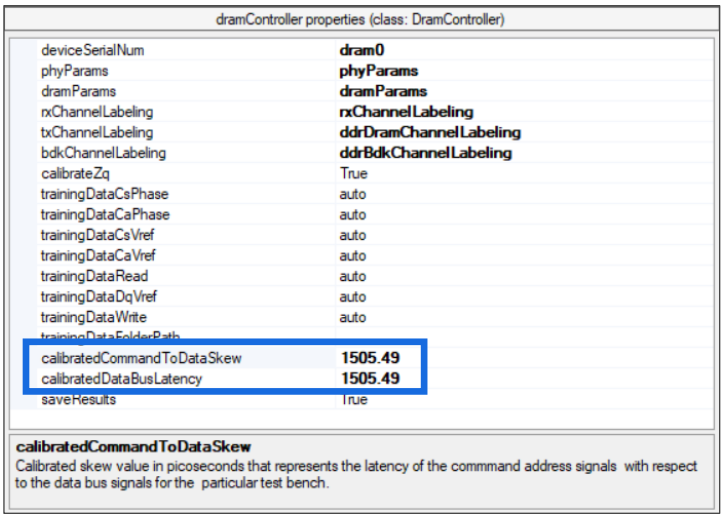


**Figure 4**: Calibration Data Fields in the DRAM Test Suite

TABLE 4: REFERENCES

| USER GUIDES | |
|---|---|
| DDR5 DRAM Test Suite User Guide | EN-G057E-E-21113 |

| Revision Number | History | Date |
|---|---|---|
| 1.0 | Document Release | April 23, 2021 |

The information in this document is subject to change without notice and should not be construed as a commitment by Introspect Technology. While reasonable precautions have been taken, Introspect Technology assumes no responsibility for any errors that may appear in this document.



Published in Canada on April 23, 2021
EN-G056E-E-21113

INTROSPECT.CA