QUICK START GUIDE

DDR5 DRAM Test Suite User Guide

C SERIES

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INTROSPECT.CA

Table of Contents

Introduction

OVERVIEW

Introspect Technology's DRAM Test Suite is the complete solution for performing device initialization and configuration, training, transmitter and receiver characterization, and functional testing on a DDR5 DRAM test bench. The test suite targets the SV5C 32 channel bidirectional system to drive the DRAM command address bus, as well as generate write traffic and capture read bursts.

QUICK START DOCUMENTATION

This Quick Start Guide will provide the information required for a user to set up the DDR5 DRAM test bench by providing detailed descriptions and diagrams for all the required connections.

HARDWARE REQUIREMENTS

- (QTY = 1) SV5C-12 32 channel bidirectional system
- (QTY = 1) 2 port programmable power supply
- (QTY = 8) Huber+Suhner MXP to SMA female cables (Introspect part # 4813)
- (QTY = 3) Huber+Suhner MXP to MXP cables (Introspect part # 4814)
- (QTY = 22) SMA male to SMA male adapters (example manufacturer part # - Amphenol RF 132168)
- (QTY = 10) 8" matched SMP to SMA cables (Introspect part # 4818)
- (QTY = 2) 50 Ohm Term (example manufacturer part # – Mini-Circuits ANNE-50+ TERM/SMA-M/18GHZ RoHS)
- (QTY = 2) DC Block (example manufacturer part # – Mini-Circuits BLK-89-S+ DC BLOCK/SMA-F/SMA-M/RoHS)
- (QTY = 1) PC for running the Introspect ESP Software

NOTE ABOUT HARDWARE

The hardware requirements list assumes the DRAM interface signals are accessible via 3 MXP connectors on the board, and cables are selected to minimize delays through the test bench. If different connectors or cables are required, please contact Introspect Technology via the Service Desk for assistance (https://introspect.atlassian.net/servicedesk/customer/portals).

Test Bench Setup

SV5C 32 CHANNEL BIDIRECTIONAL SYSTEM

The SV5C 32 channel bidirectional system requires a special form factor, and it also requires unique connections between the two SV5C units for synchronization. Follow the instructions in the document "EN-G045E-E-20078 SV5C 32 Channel Quick Start Guide", using the provided form factor folder "SV5C_32C12G_BIDIR_DDR" in place of the one referenced in the document ("SV5C_32C12G_DDR"). The SV5C units will be hereafter referred to as Box 1 and Box 2, as per the definition in the above-mentioned document.

SV5C BIDIRECTIONAL KIT CONTROL BUS

The SV5C Bidirectional Kit control bus is connected to the Box 1 SV5C, as shown in Figure 1.

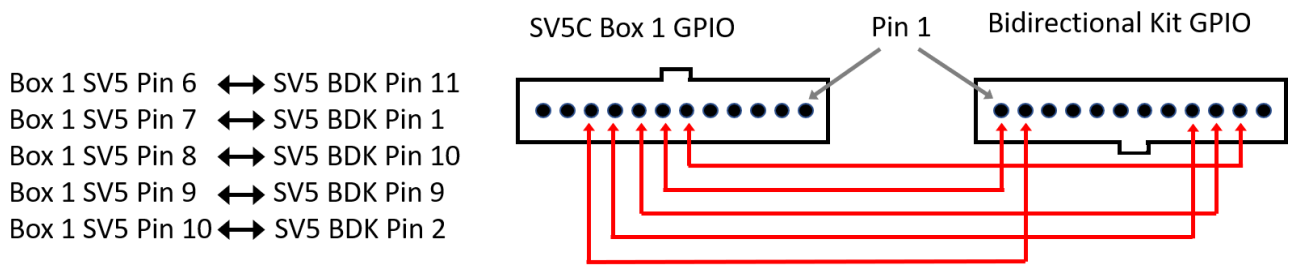

Figure 1: Pin diagram of SV5C to SV5C Bidirectional Kit GPIO jumper cables

POWER SUPPLY

The power requirement is specific to the test board that is used, but typically there are two supply channels at 1.8V and 1.1V for the VPP and VDD power rails. Connect the channels, ensuring the polarity of the supplies are correct, and connect all the grounds.

DRAM COMMAND ADDRESS BUS

Refer to Table 1 and Table 2 for the mapping of the SV5C channels to the pins on the test board. For a mapping of the SV5C channel numbers to pin numbers on the MXP connectors, refer to the SV5C data sheet listed in the references section at the end.

TABLE 1: SV5C TX CHANNEL TO DRAM SIGNAL MAPPINGS

SV5C CHANNEL	DRAM SIGNAL NAMES
TX1P	CK_T
TX1N	CK_C
TX2P	RST
TX3P	CSN
TX4P	CA0
TX5P	CA1
TX6P	CA2
TX7P	CA3
TX8P	CA4
TX9P	CA5
TX10P	CA6
TX11P	CA7
TX12P	CA8
TX13P	CA9
TX14P	CA10
TX15P	CA11
TX16P	CA12
TX17P	CA13
TX18P	TDQSt/DM
TX19P	TDQSc

TABLE 2: SV5C RX CHANNEL TO DRAM SIGNAL MAPPINGS

SV5C CHANNEL	DRAM SIGNAL NAMES
RX1P	LBDQ
RX1N	Connect to DC block and 50 Ohm term
RX2P	LBDQS
RX2N	Connect to DC block and 50 Ohm term

DRAM DATA BUS

Refer to Table 3 for a mapping of the SV5C channels to the SV5C Bidirectional Kit (BDK) and to the pins on the test board.

TABLE 3: SV5C BIDIRECTIONAL KIT TO DRAM SIGNAL MAPPINGS

SV5C CHANNEL	BOX 2 CHANNEL	BDK MXP CHANNEL	BDK SMP CHANNEL	DRAM SIGNAL NAME
TX21P	TX5P	TX1P	DUT1	DQST
TX21N	TX5N	TX1N	-	-
RX21P	RX5P	RX1P	-	-
RX21N	RX5N	RX1N	-	-
TX22P	TX6P	TX2P	DUT2	DQSC
TX22N	TX6N	TX2N	-	-
RX22P	RX6P	RX2P	-	-
RX22N	RX6N	RX2N	-	-
TX23P	TX7P	TX3P	DUT3	DQ0
TX23N	TX7N	TX3N	-	-
RX23P	RX7P	RX3P	-	-
RX23N	RX7N	RX3N	-	-
TX24P	TX8P	TX4P	DUT4	DQ1
TX24N	TX8N	TX4N	-	-
RX24P	RX8P	RX4P	-	-

RX24N	RX8N	RX4N	-	-
TX25P	TX9P	TX5P	DUT5	DQ2
TX25N	TX9N	TX5N	-	-
RX25P	RX9P	RX5P	-	-
RX25N	RX9N	RX5N	-	-
TX26P	TX10P	TX5P	DUT6	DQ3
TX26N	TX10N	TX5N	-	-
RX26P	RX10P	RX5P	-	-
RX26N	RX10N	RX5N	-	-
TX27P	TX11P	TX6P	DUT7	DQ4
TX27N	TX11N	TX6N	-	-
RX27P	RX11P	RX6P	-	-
RX27N	RX11N	RX6N	-	-
TX28P	TX12P	TX7P	DUT8	DQ5
TX28N	TX12N	TX7N	-	-
RX28P	RX12P	RX7P	-	-
RX28N	RX12N	RX7N	-	-
TX29P	TX13P	TX8P	DUT9	DQ6
TX29N	TX13N	TX8N	-	-
RX29P	RX13P	RX8P	-	-
RX29N	RX13N	RX8N	-	-
TX30P	TX14P	TX9P	DUT10	DQ7
TX30N	TX14N	TX9N	-	-
RX30P	RX14P	RX9P	-	-
RX30N	RX14N	RX9N	-	-

TEST BENCH CONNECTION DIAGRAM

Figure 2 shows a complete diagram of the SV5C 32 channel bidirectional system for DRAM testing.

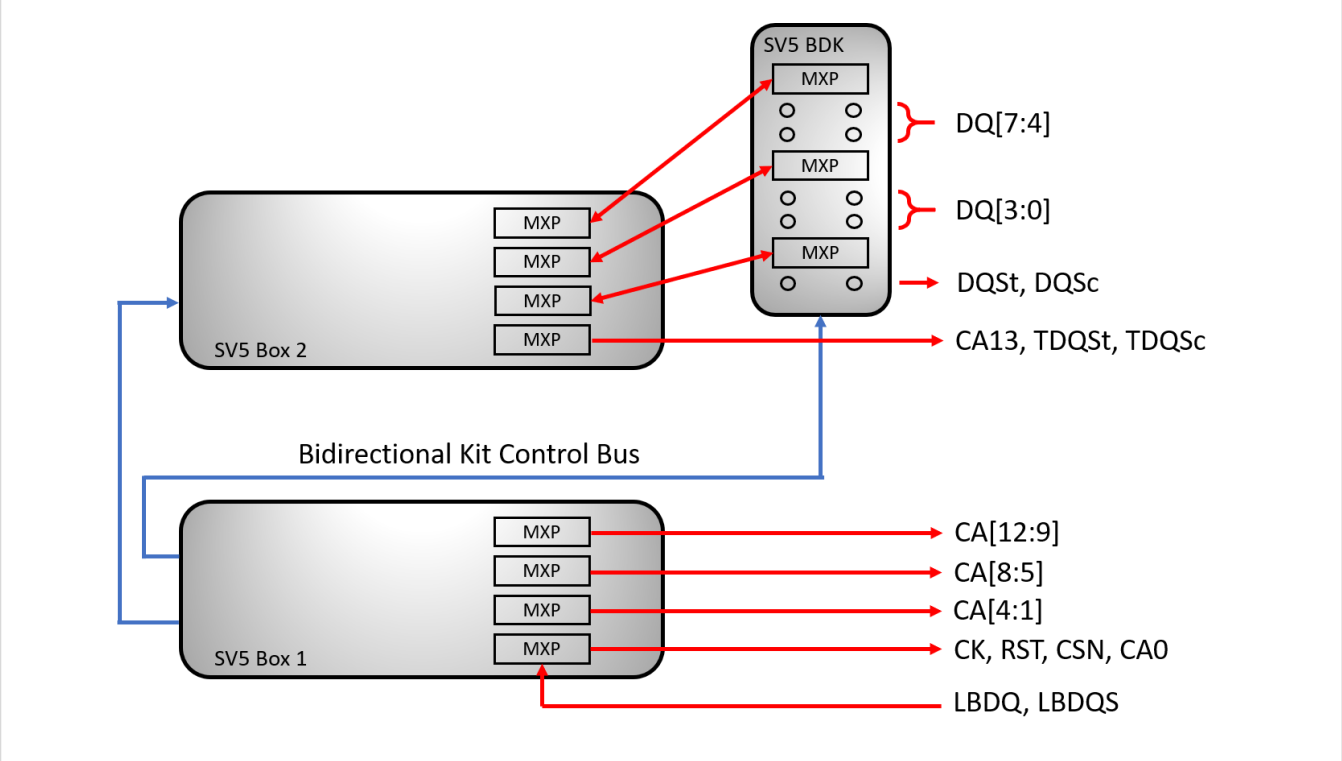

Figure 2: SV5C 32 Channel Bidirectional System for DRAM Testing

Using the DRAM Test Suite

NOTE ON SOFTWARE VERSION

The version of the Introspect software that should be used will depend on the version of the DRAM Test Suite. Please contact Introspect Technology via the Service Desk for this information (https://introspect.atlassian.net/servicedesk/customer/portals).

GETTING STARTED

USING THE INTROSPECT GUI

Open the test suite in the Introspect ESP Software GUI with the "SV5C_32C12G_BIDIR_DDR" form factor as in Figure 3.

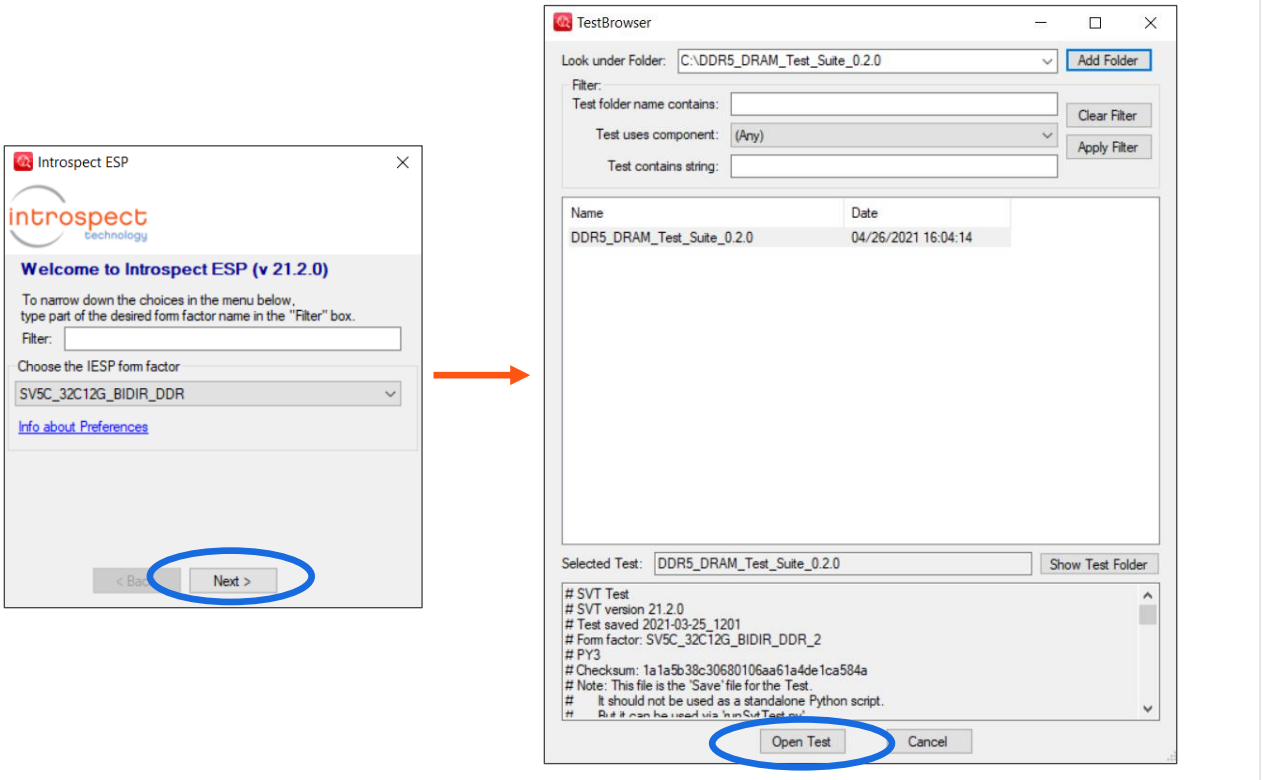

Figure 3: Opening the DRAM Test Suite in the Introspect ESP Software GUI

USING AN EXTERNAL PYTHON SCRIPT

The DRAM Test Suite functionality may be accessed from an external python script by following the steps below:

1. Install the correct Python version and modules, by referring to the sections "Python Version" and "Required Python Modules" in the document "UsingComponentsInExternalPythonScripts.pdf". This document can be found inside the Introspect GUI under *Help->Application Notes->Script User Manual.*

2. Edit the python module search path in "dramTestSuiteScript.py" (located in the *TestAsPythonScript* subfolder of the test suite) to point to *SvtPython* in the Introspect GUI installation folder

   ```
   svtPythonPath = <iespInstallPath>\SvtPython
   ```

   and edit the FTDI serial numbers to match those in the custom form factor file "Documents\Introspect\Config\CustomFormFactors\SV5C_32C12G_BIDIR_DDR\config.csv".

   ```
   ftdiSerialNums = ['FTDI:INSV5M20050020A', 'FTDI:INSV5M20050020B',
   'FTDI:INSV5M19110010A', 'FTDI:INSV5M19110010B']
   ```

   Alternatively, both these steps can be performed automatically by opening the test procedure in the Introspect GUI and clicking *File->Save*.

3. The DRAM Test Suite functionality can now be used externally by importing the test suite module as below.

   ```
   import sys
   testSuitePath = r'<ddr5DramTestSuitePath>\TestAsPythonScript'
   sys.path.append(testSuitePath)
   import dramTestSuiteScript
   ```

TEST SUITE CODE

The DRAM Test Suite provides everything required for performing transmitter and receiver characterization and functional testing on a DRAM, including the steps to initialize the device and bring it to a functional state. The pre-built functions defined in "dramTestSuite.py" in the *PythonCode* folder of the test procedure, along with the *DdrDramController* component in the Introspect ESP software, can be used to build a custom test script that exercises the DRAM device under test. A simple example of such a test script is shown in Figure 4.

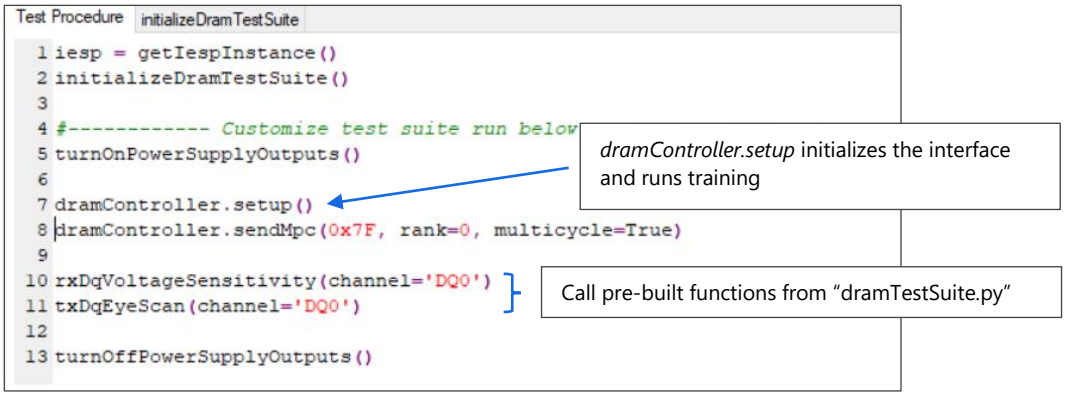

Figure 4: Example Test Procedure Using the DDR5 DRAM Test Suite

DRAM CONTROLLER

The *DdrDramController* component class provides an interface for communicating with the DRAM device under test. It handles all initialization, configuration, and training of the DRAM, as well as providing a simple API for sending test patterns and commands. The software also provides several parameter components that can be linked to the *DdrDramController* to customize the DRAM interface, as in Figure 5. The full API documentation for the *DdrDramController* and other related components can be found inside the Introspect GUI under *Help->Component Classes.*

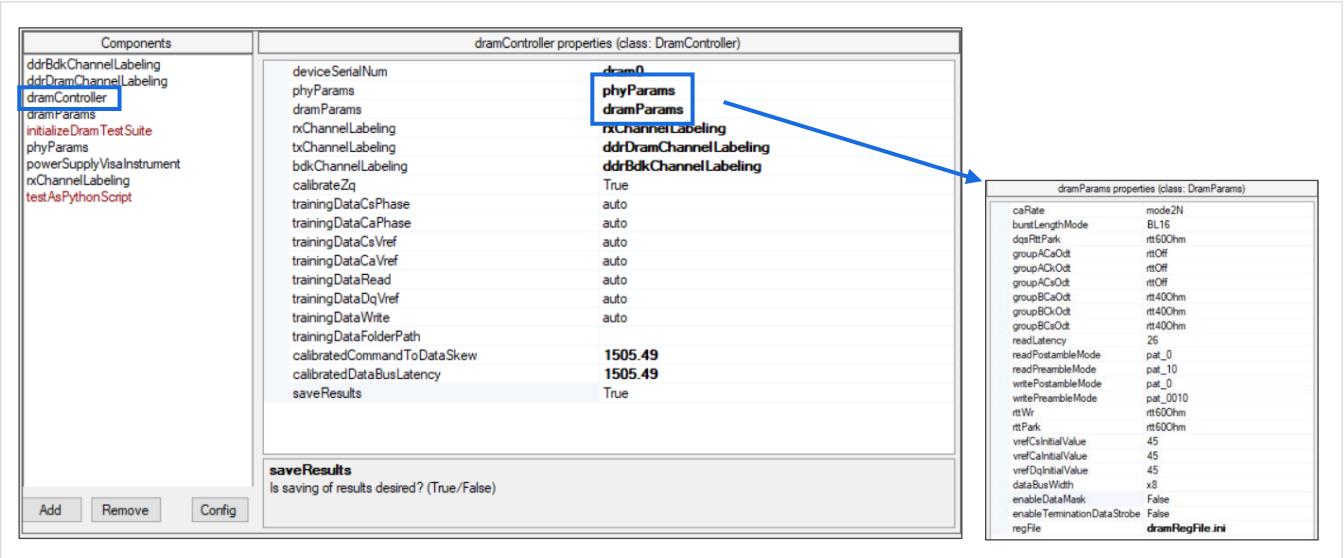

Figure 5: Customizing the DRAM controller interface

Summary

This document described the Introspect Technology DRAM Test Suite, which is a complete solution for testing and training a DDR5 DRAM device under test. It enables performing device initialization and configuration, training, transmitter and receiver characterization, and functional testing on a DDR5 DRAM test bench. The document described the hardware connection diagrams in detail and provided simple step-by-step instructions to starting the test suite and using it.

TABLE 4: REFERENCES

DATA SHEET	
SV5C Data Sheet	MK-D014E-E-20063
USER GUIDES	
SV5C 32 Channel Quick Start Guide	EN-G045E-E-20078

Revision Number	History	Date
1.0	Document Release	April 23, 2021

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