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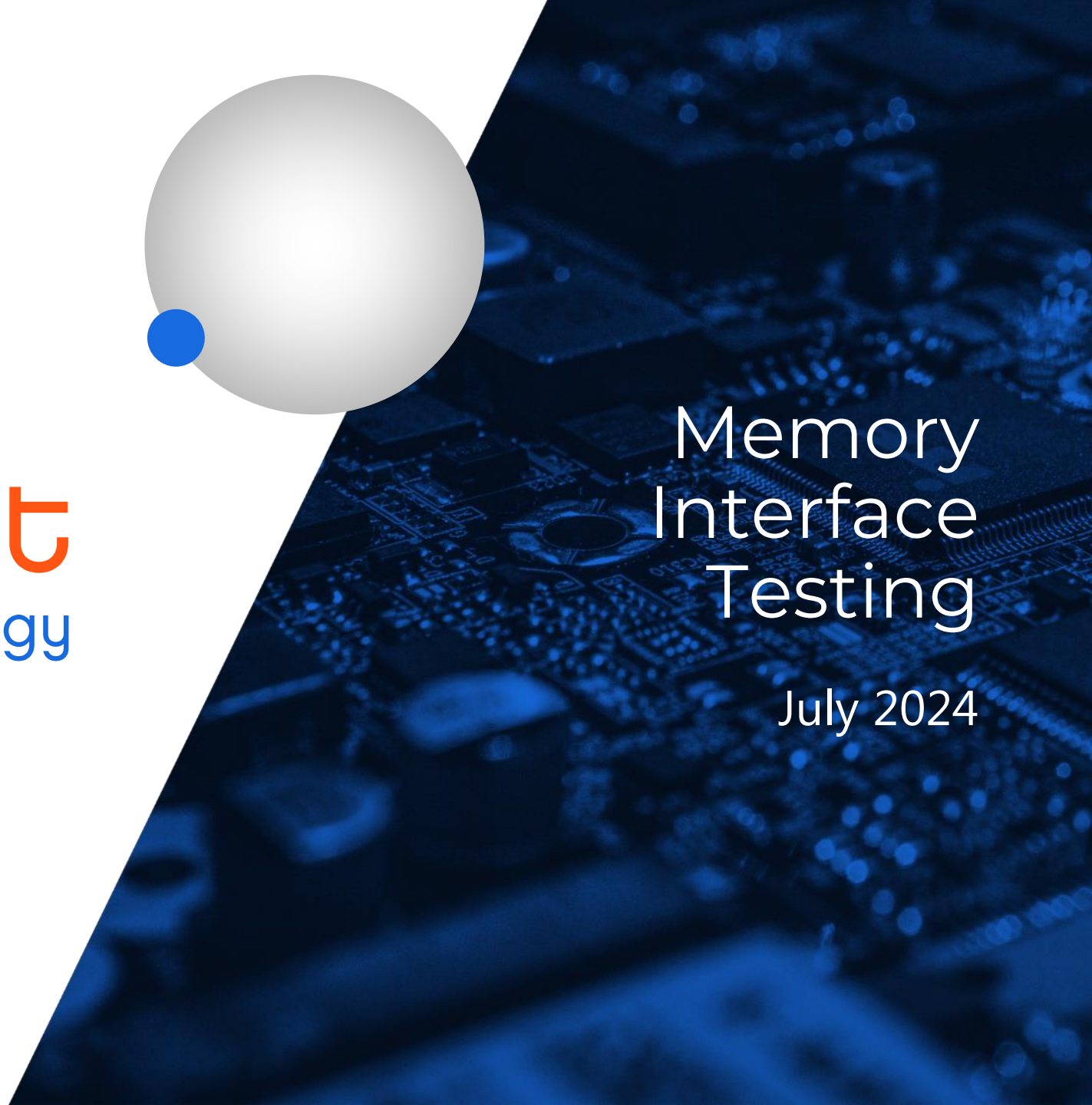
Memory Interface Testing

July 2024



Agenda

1. About Introspect Technology
2. Scope of This Presentation
3. ATE on Bench Architecture
4. Memory and Component Testing
5. Host Controller Testing
6. Protocol Analyzer and Interposer Systems
7. SV6E-X SidebandBus Controller and Tester
8. Summary

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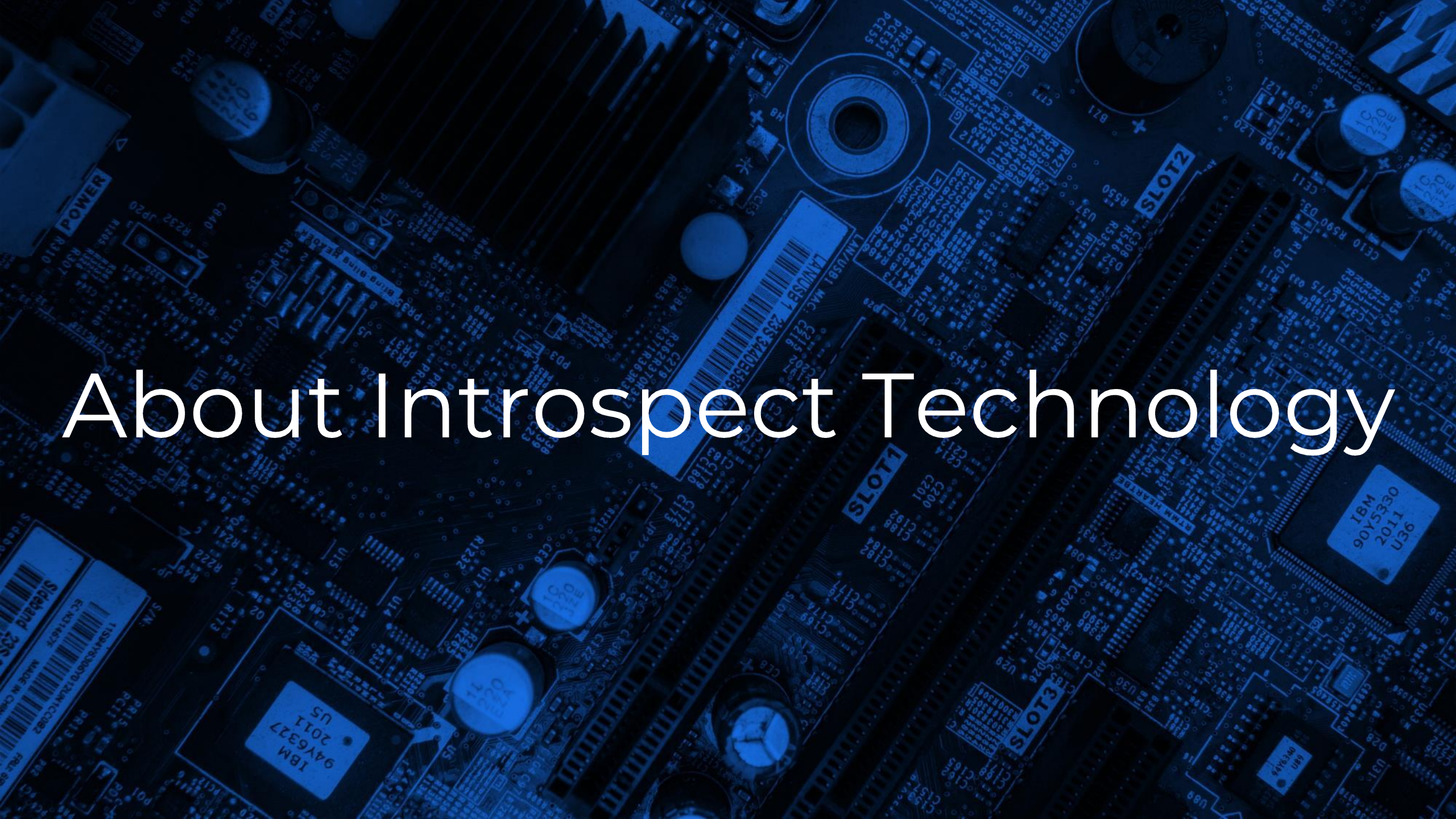

About Introspect Technology

Introspect Makes Tools for Engineers

ADDRESSING GAP IN TEST EQUIPMENT AVAILABILITY

Bench

ATE

~~Costly, few lanes, slow~~

~~Rigid, low performance~~

- Bench-like accuracy and precision
- EDA style scripting
- Software-style regression and versioning
- ATE-like speed
- Highly parallel
- Designed for automation

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We Test Electronic Interfaces…

IR RANGE FINDERS

IMAGE SENSORS

DISPLAYS

MOTION SENSORS, MICROPHONES, SPEAKERS

POWER MANAGEMENT ICs

APPLICATIONS PROCESSORS

MEMORIES

RF ICs

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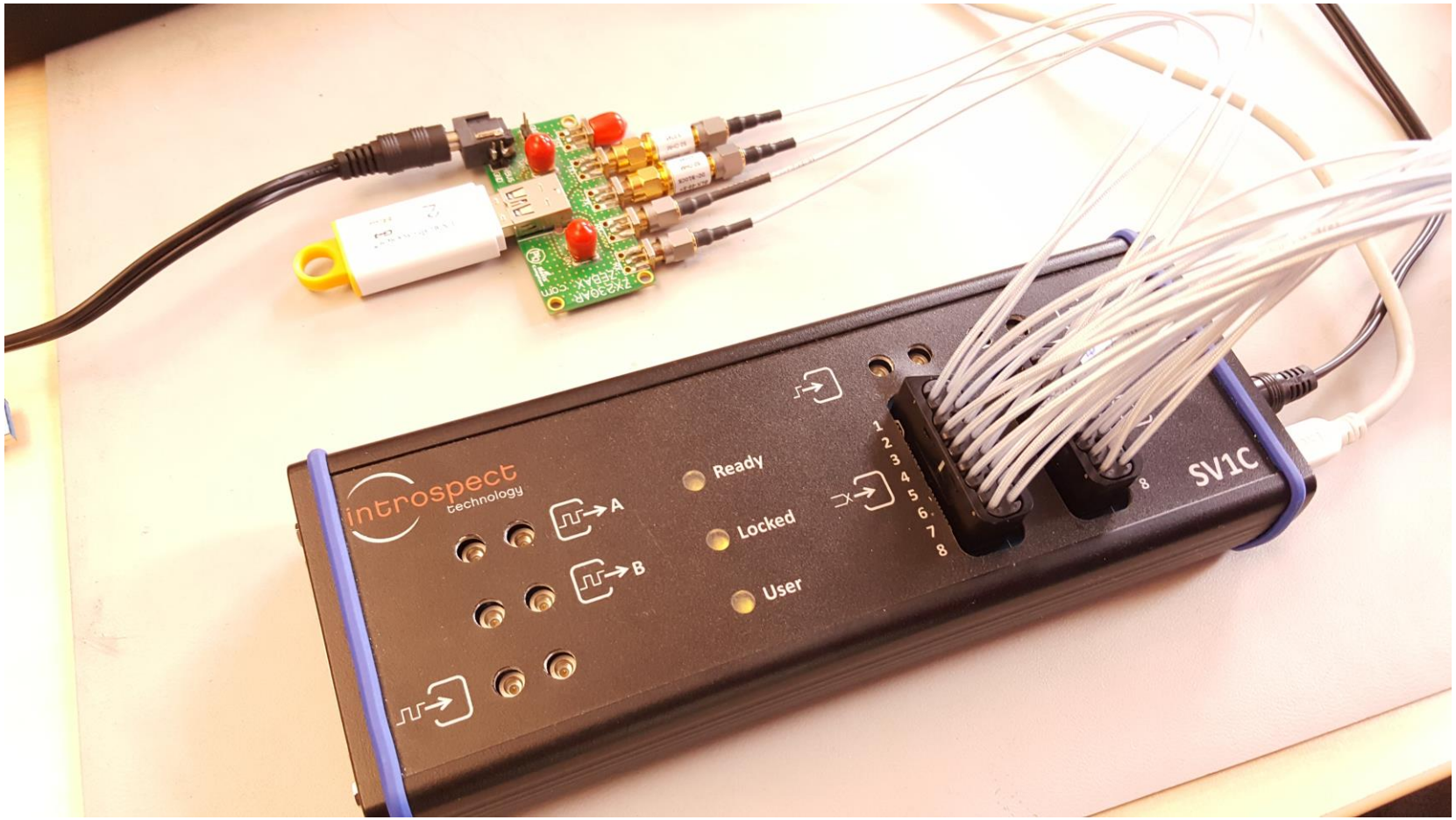
We Act as a Link Partner / Exerciser…



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And We Probe a Live System

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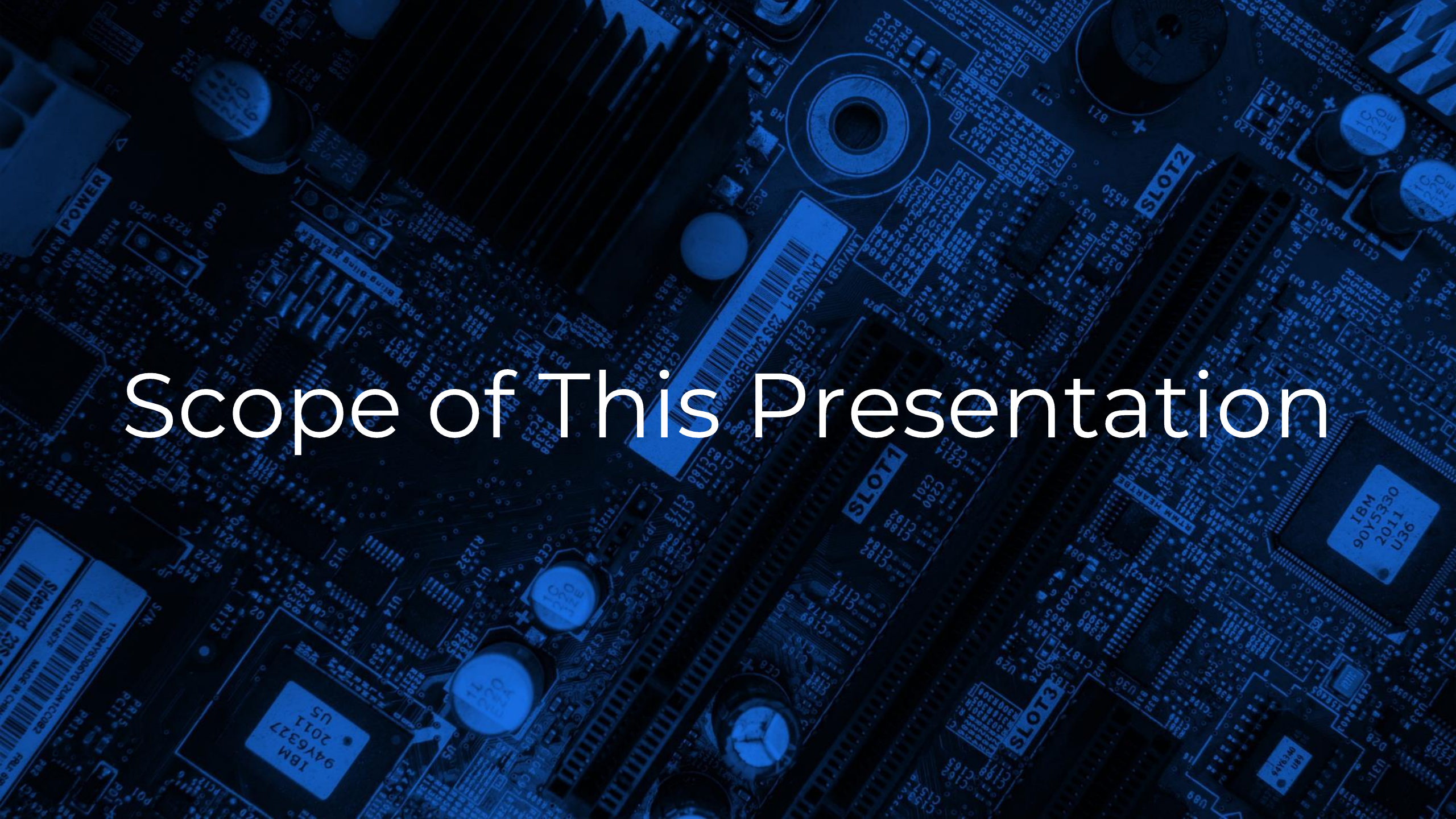
Company Facts

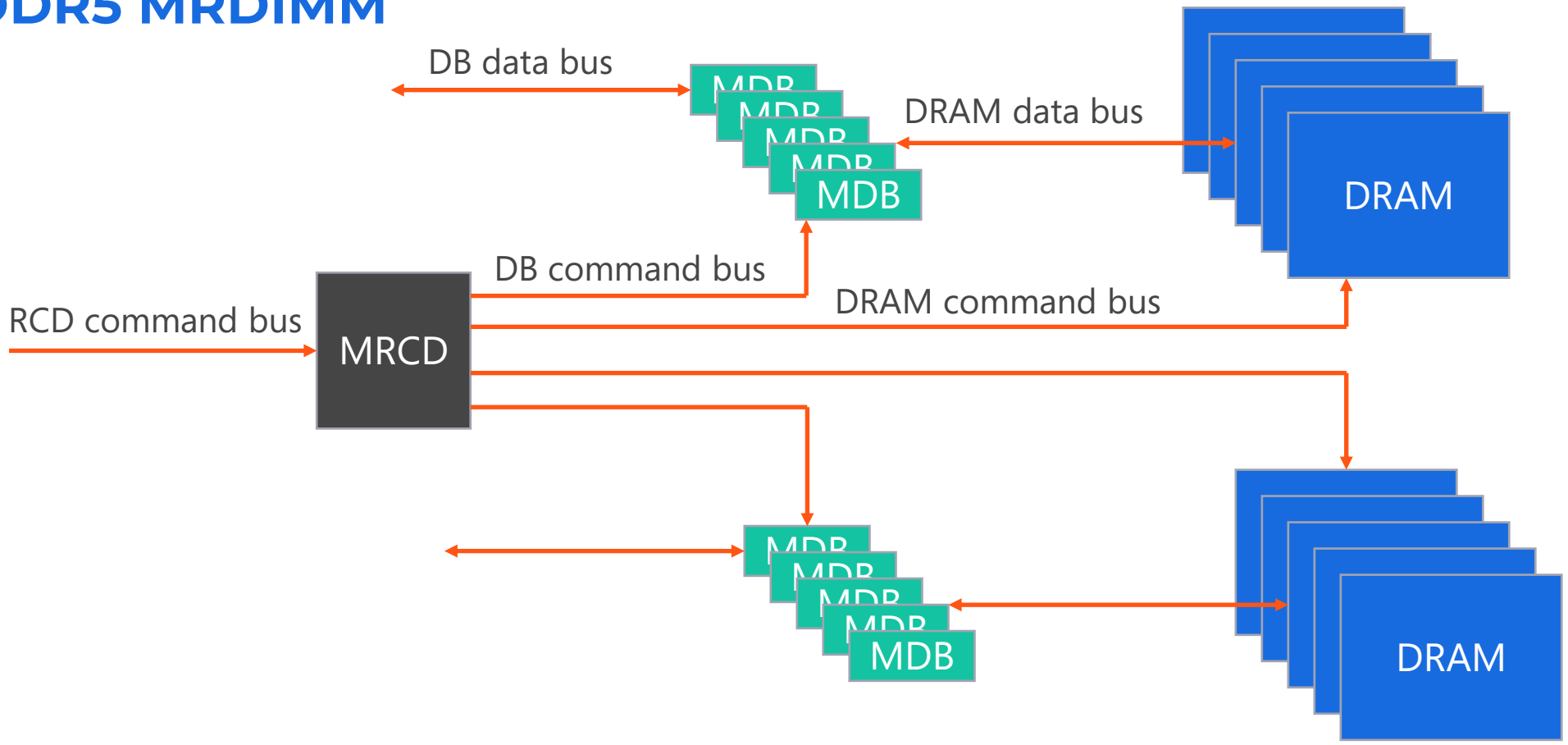
- Founded in 2012
- Offices in Montréal, Québec and Vancouver, British Columbia
- Global, outsourced sales and distribution channel
- Manufacturer of capital equipment used in the design validation and mass production testing of electronic components that contain high-speed communications interfaces
  - Smartphones
  - Personal computers and tablets
  - Augmented reality headsets
  - Automotive systems and self-driving systems
  - Data center server racks
  - Medical equipment



Scope of This Presentation

Validating Memory Interfaces

DDR5 MRDIMM



Using the above typical DDR5 DIMM architecture, we will highlight the memory interfaces that are tested by Introspect Technology

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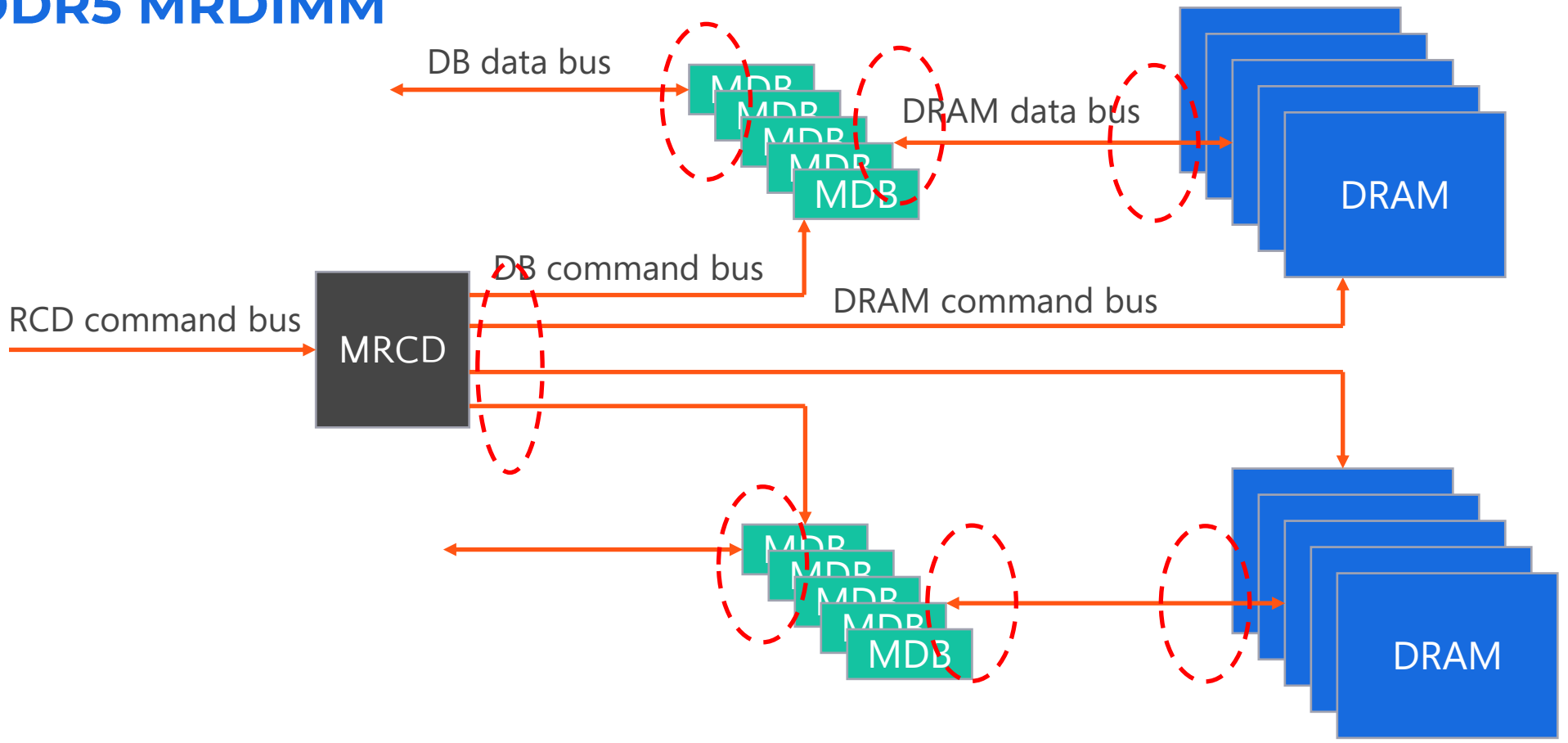
Transmitter Interfaces

DDR5 MRDIMM



Tx pins on components like RCD, DRAM, and DB

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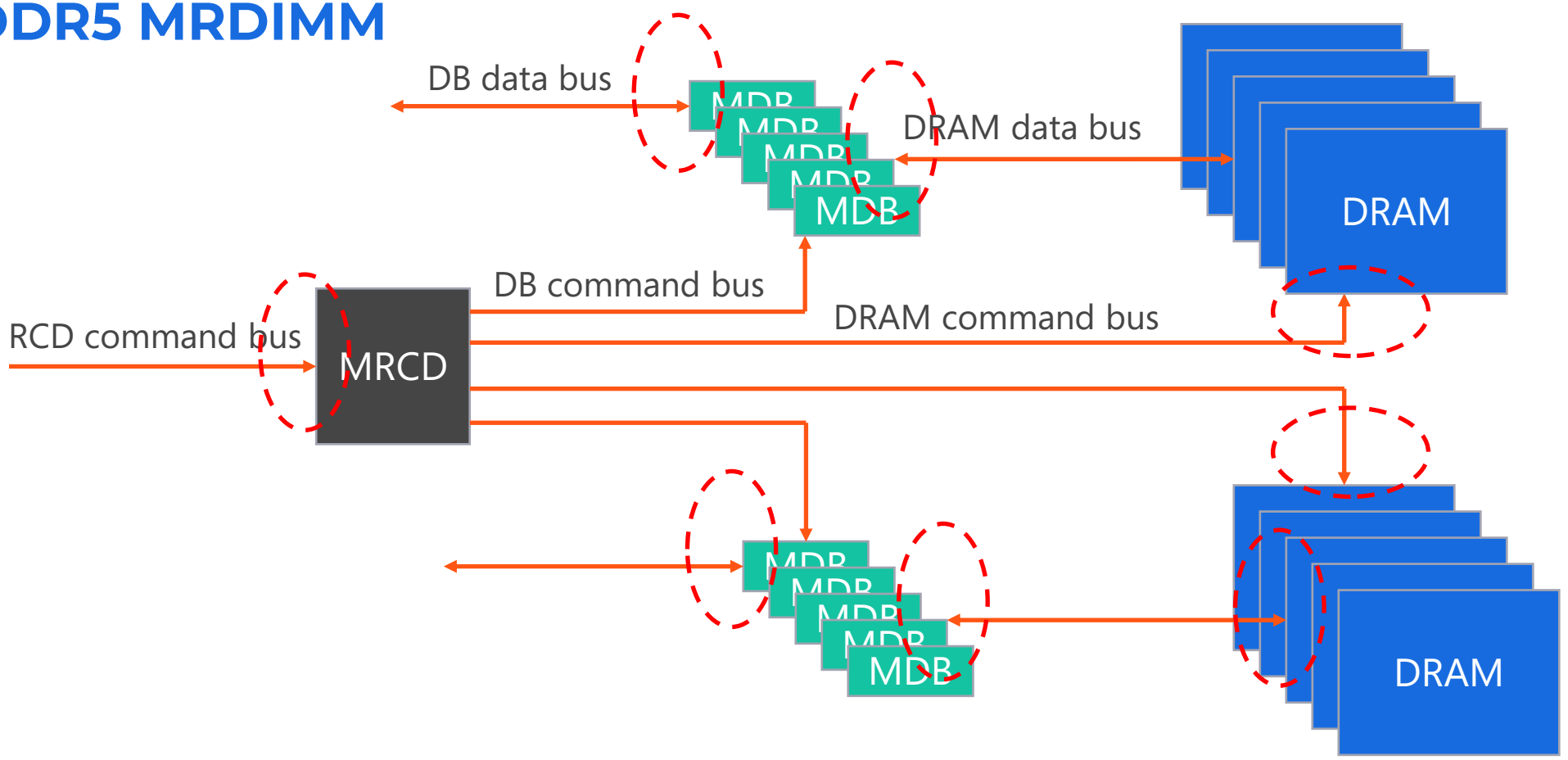
Receiver Interfaces

DDR5 MRDIMM



Rx pins on components like RCD, DRAM, and DB

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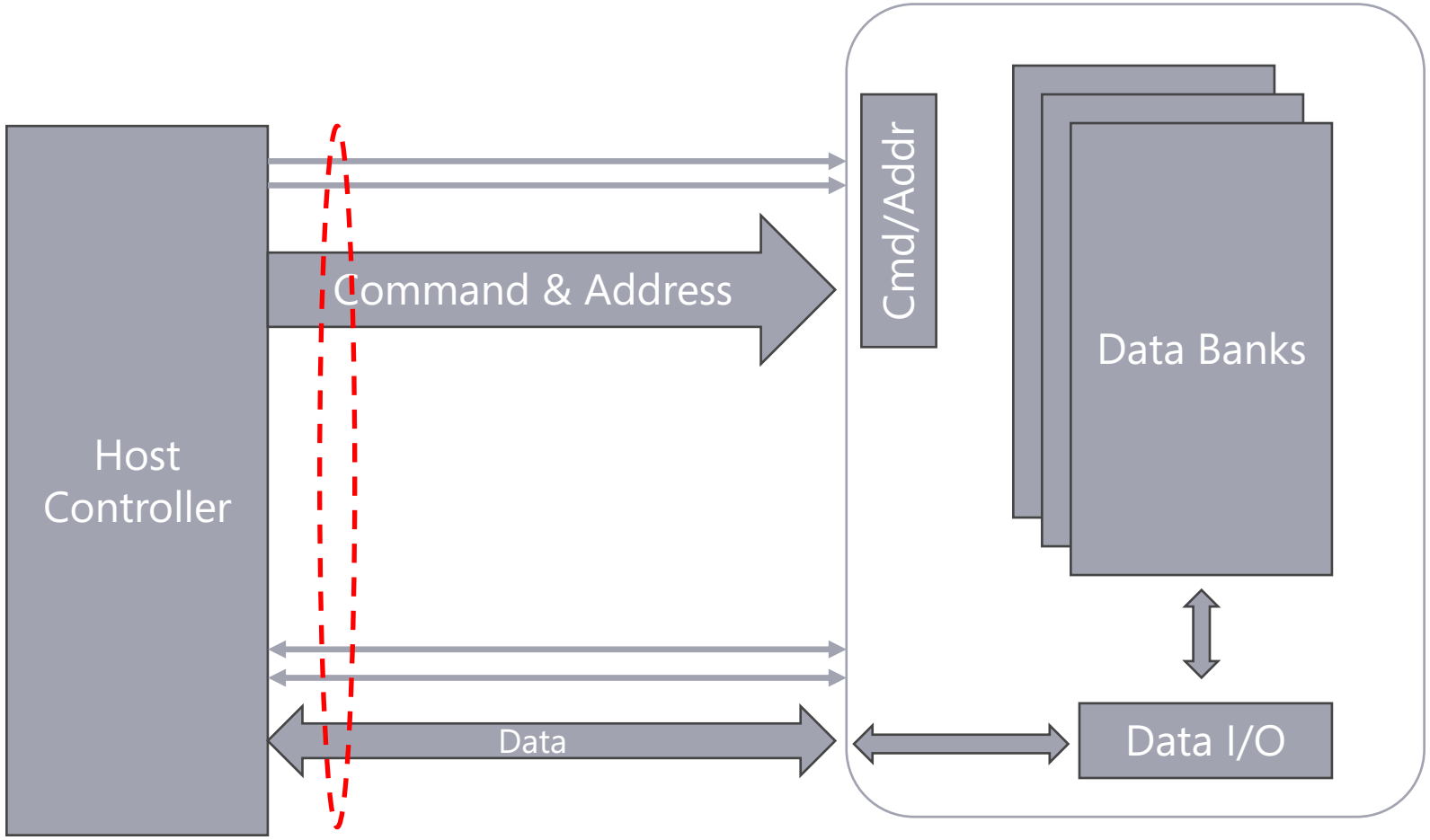
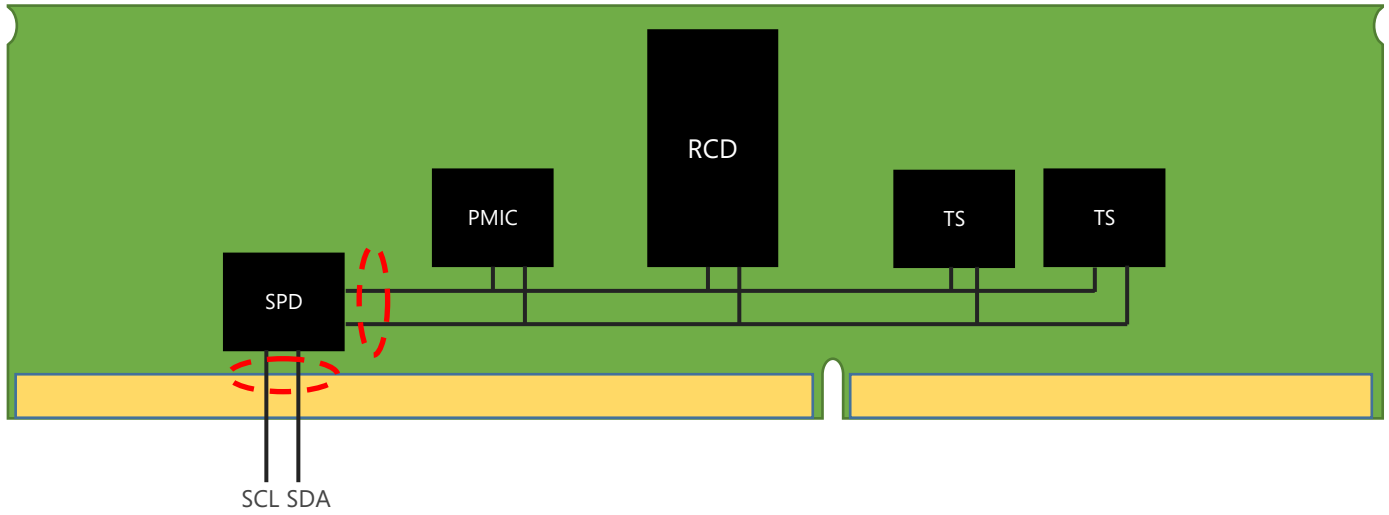
Validating Controller Components

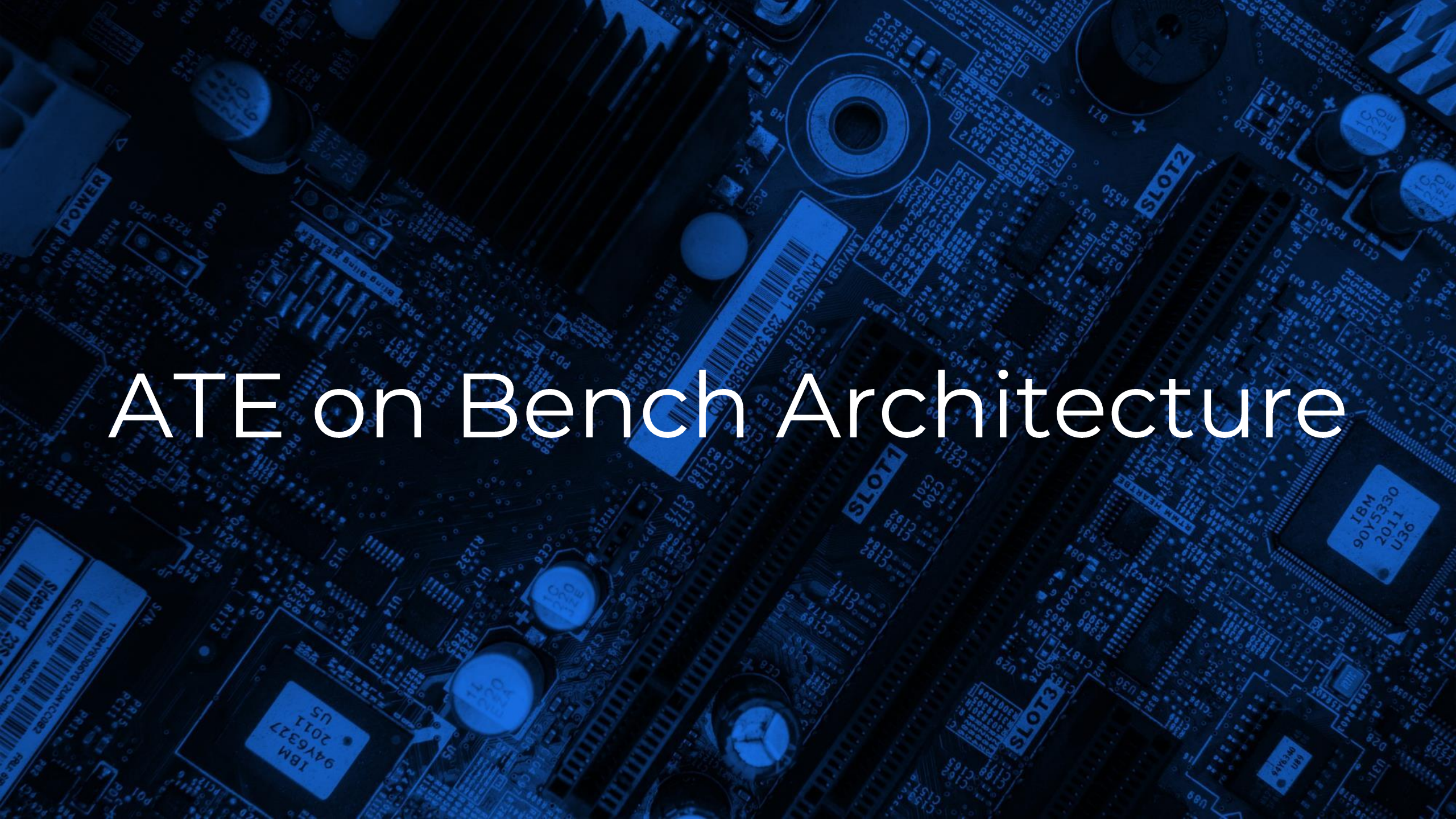


Tx and Rx pins on memory controller devices

Validating SidebandBus Components



All I2C/I3C interfaces on both the host bus and the local bus


ATE on Bench Architecture

Really Replace the ATE for DDR Testing

Complete training, shmooing capability on all pins

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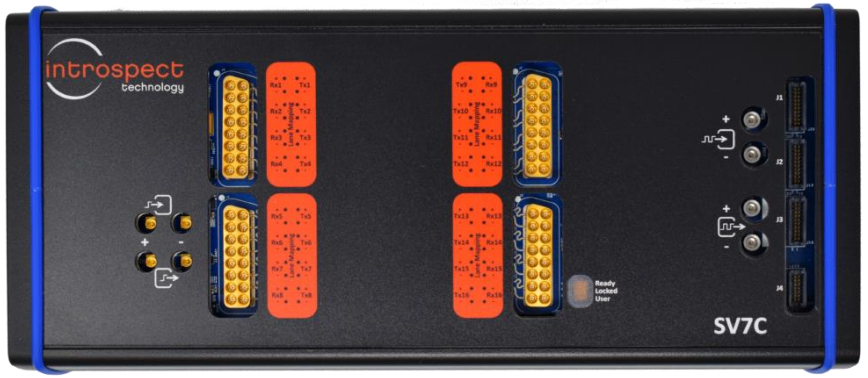
SV7C-17 ATE on Bench

DEVELOPED FOR DDR/LPDDR/GDDR INTERFACE TESTING



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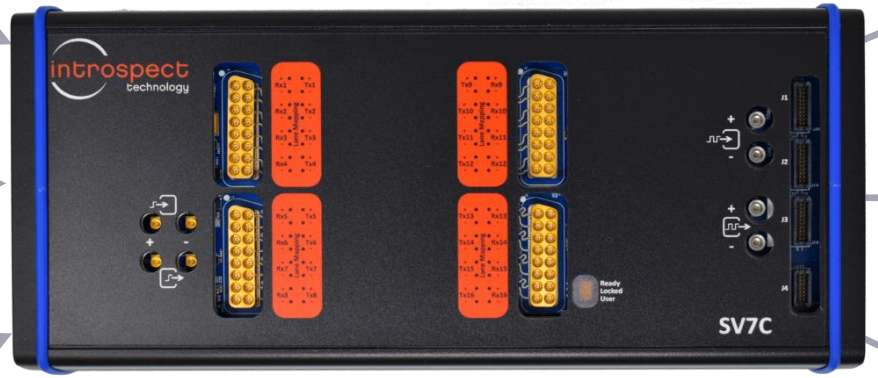
ATE on Bench

DEVELOPED FOR DDR/LPDDR/GDDR INTERFACE TESTING

CAPTURE AND ANALYSIS
Eye diagrams and BER
Parallel digital capture
Analog capture

16 RX CHANNELS
Per lane phase control
Per lane voltage threshold

16 ALIGNED RECEIVERS
capable of measuring tx skew



AUXILIARY GPIO
Provides a host of secondary controls (e.g. triggers, flags)

16 TX CHANNELS
Per lane jitter and noise injection
Per lane slew rate settings
Per lane skew control
Per lane voltage control

16 PATTERN GENERATORS
Aligned on power up
Protocol-configurable

introspect technology

ATE on Bench

DEVELOPED FOR DDR/LPDDR/GDDR INTERFACE TESTING

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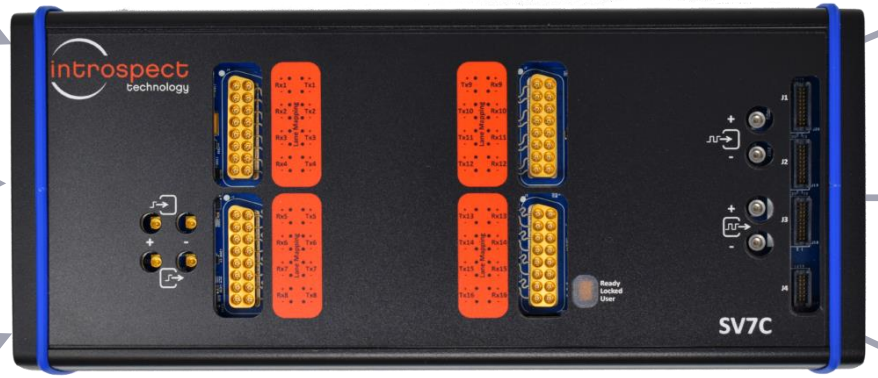

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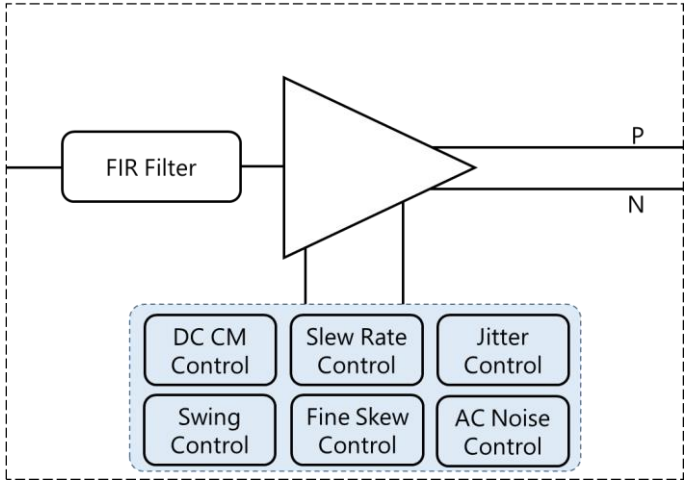
Single-Lane Pin Electronic Driver



Clock Synthesizer

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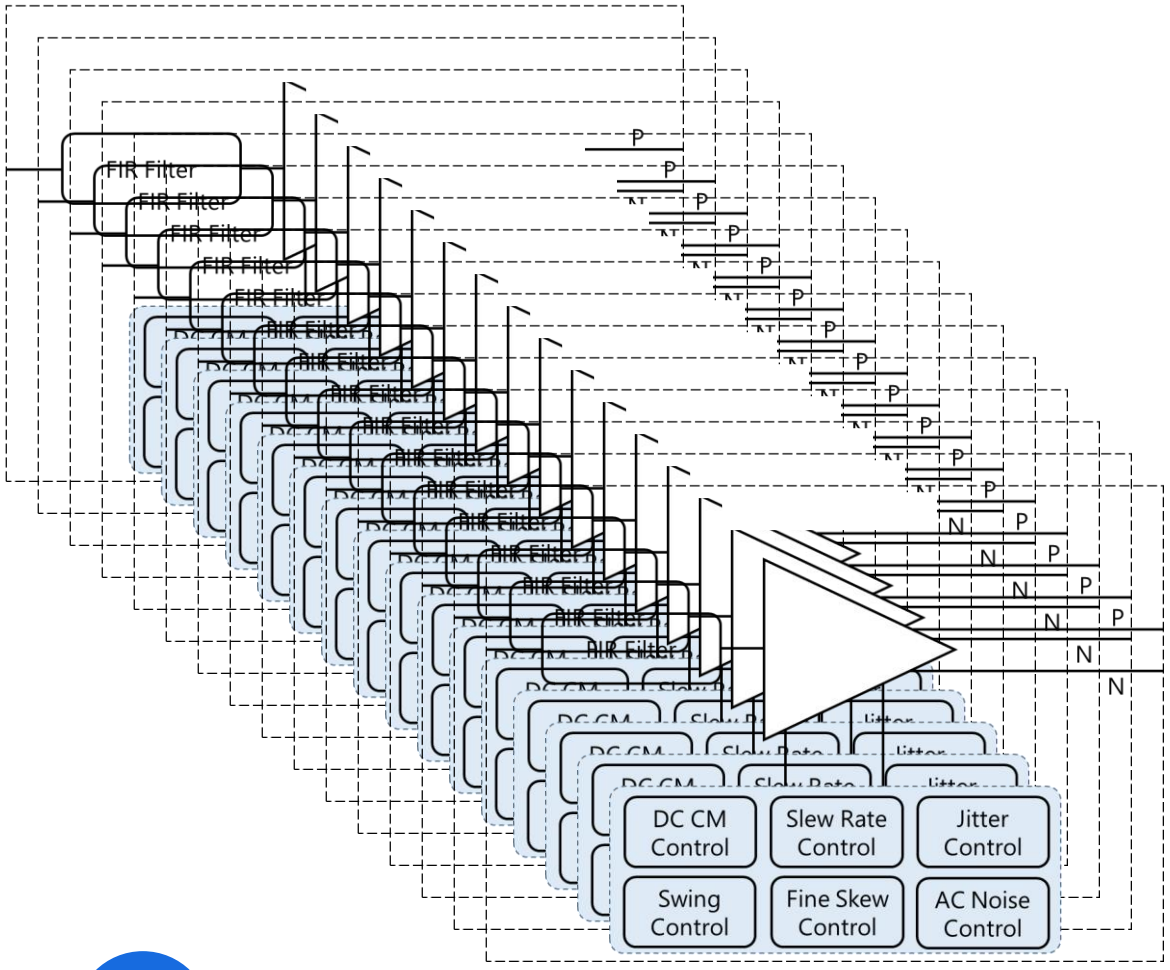
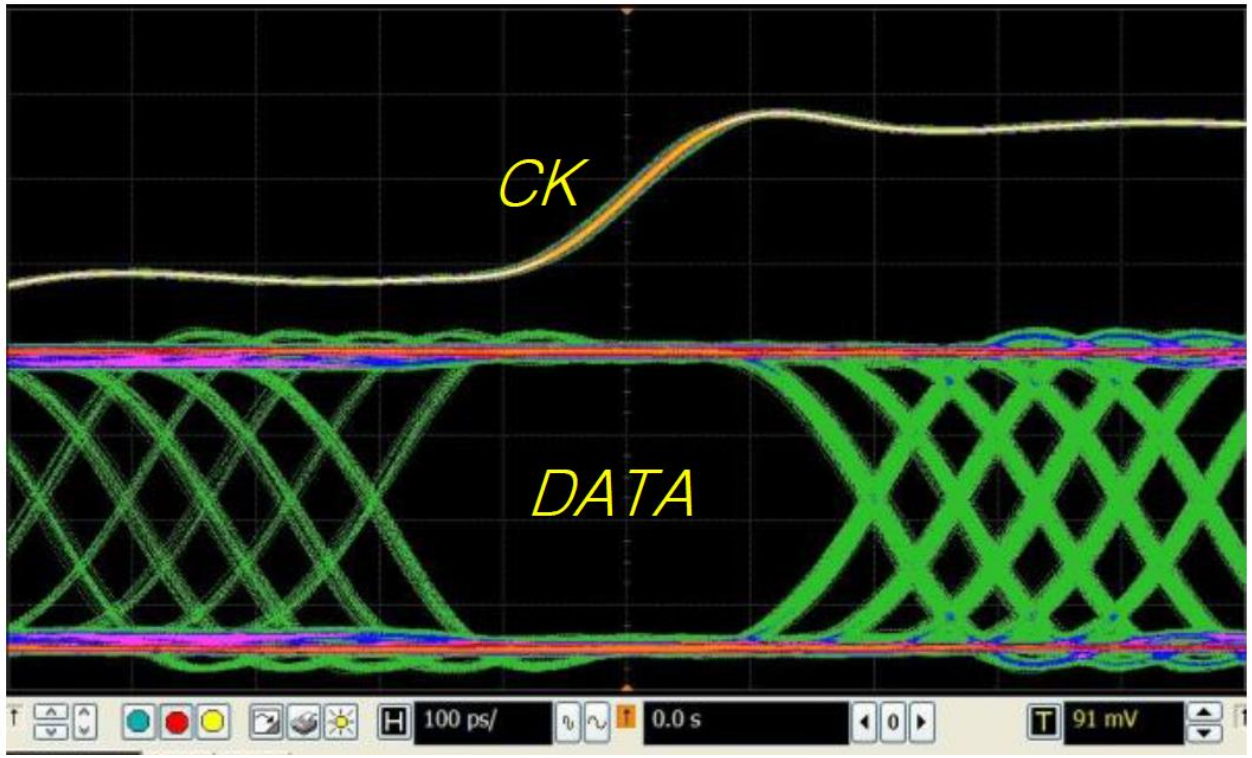
All Drivers Work as a Bus





Can produce realistic DDR/LPDDR waveform shapes & skews

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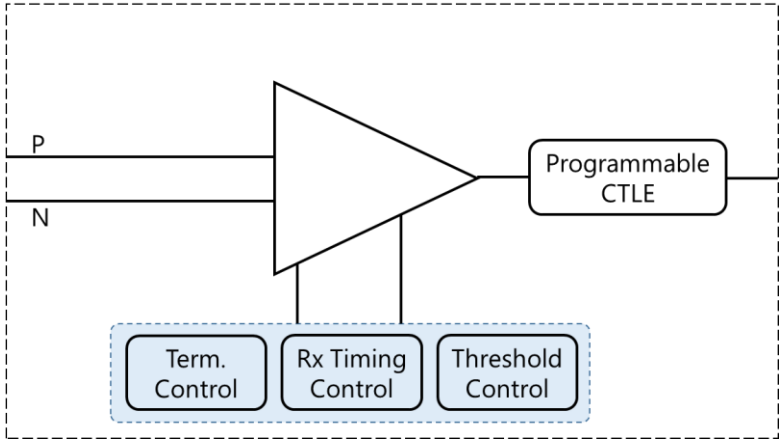
Single-Lane Pin Electronic Receiver



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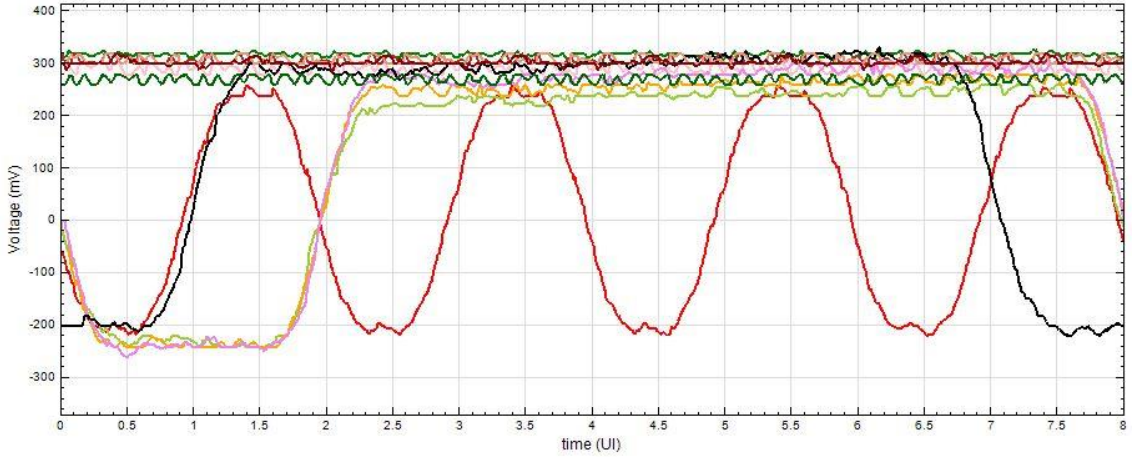
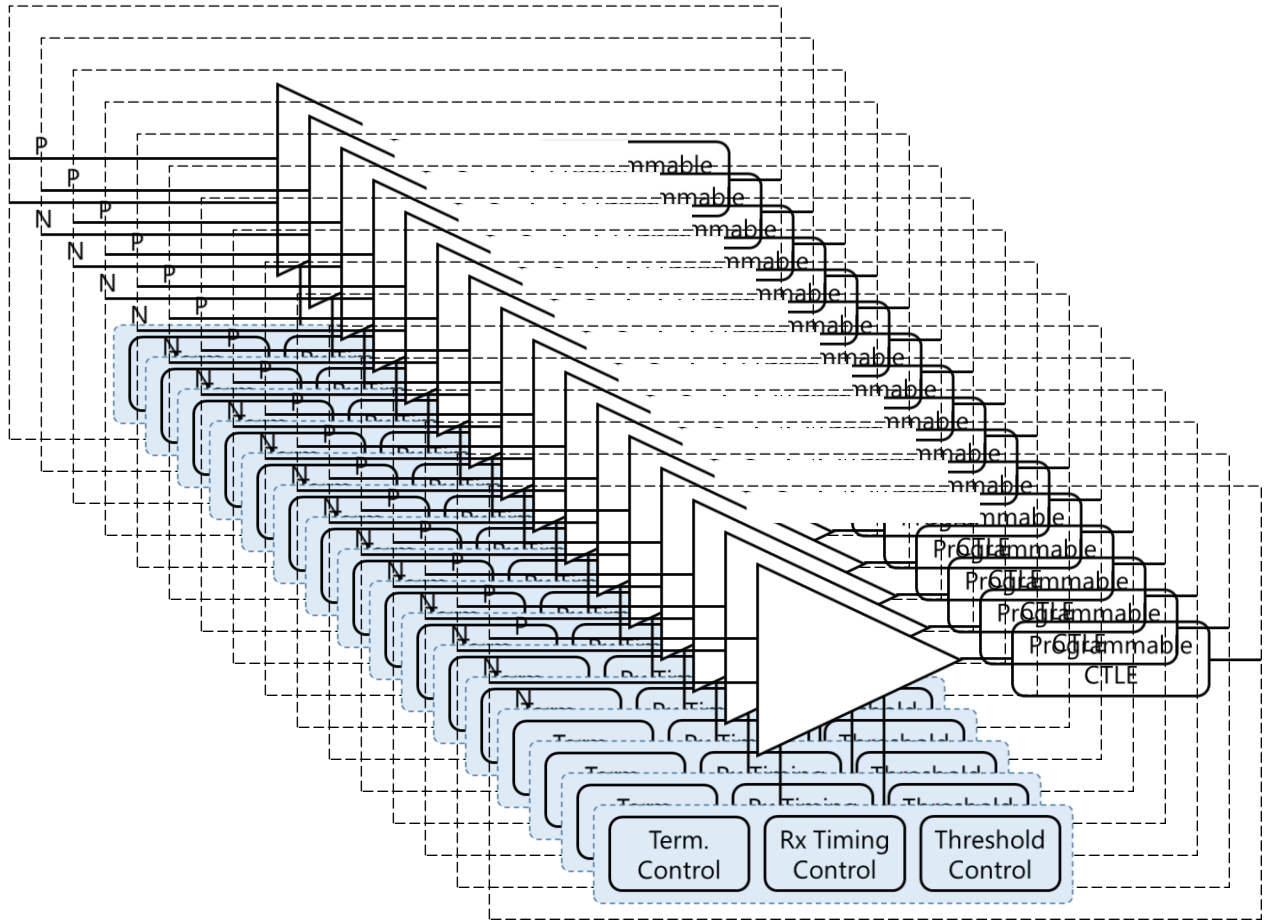
All Receivers Work as a Bus





Can capture complete bus behavior (digital and analog)

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Size Illustration (DDR and GDDR Component or PHY Test)

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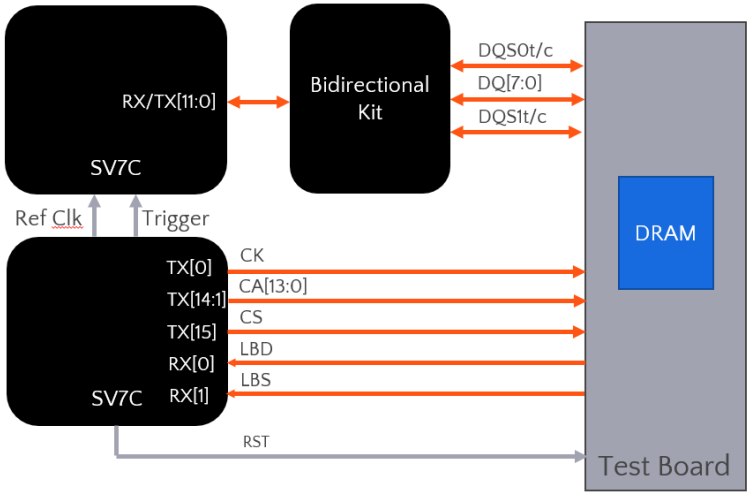
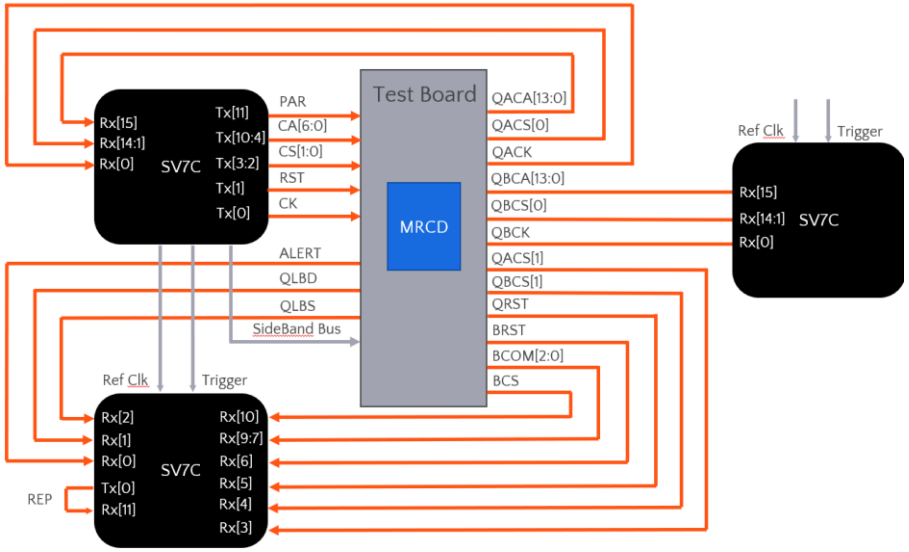
Typical DDR5 Test Benches

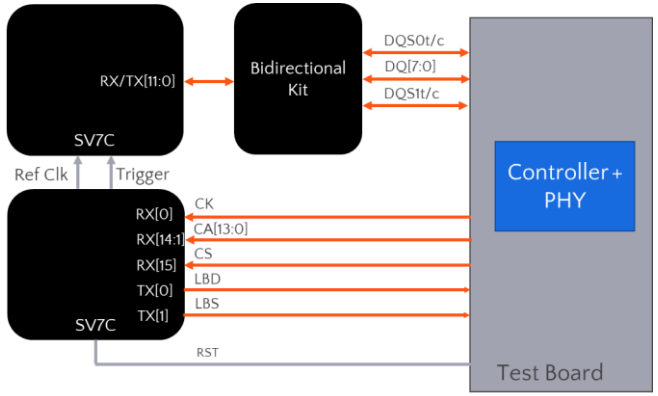
DRAM



MRCD/RCD



CONTROLLER



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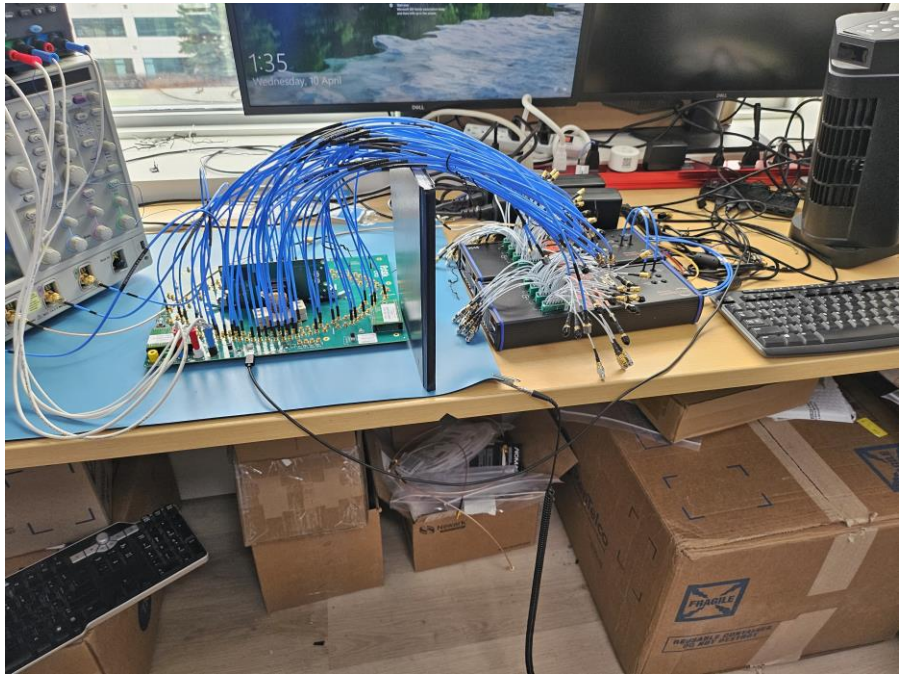
Evolution to HS Memory ATE – M Series



DDR5 RDIMM Setup

Enclosed System to Hide the
Cables and Increase Performance

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M Series Variants

COMPONENT TESTER

GDDR7 PAM3

World-first PAM3 interop test on February 7, 2024 (with leading memory maker)

COMPONENT TESTER

LPDDR5/LPDDR6

MODULE TESTER

DDR5 MR-DIMM / SO-DIMM / U-DIMM

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Example: GDDR7 4-Channel System

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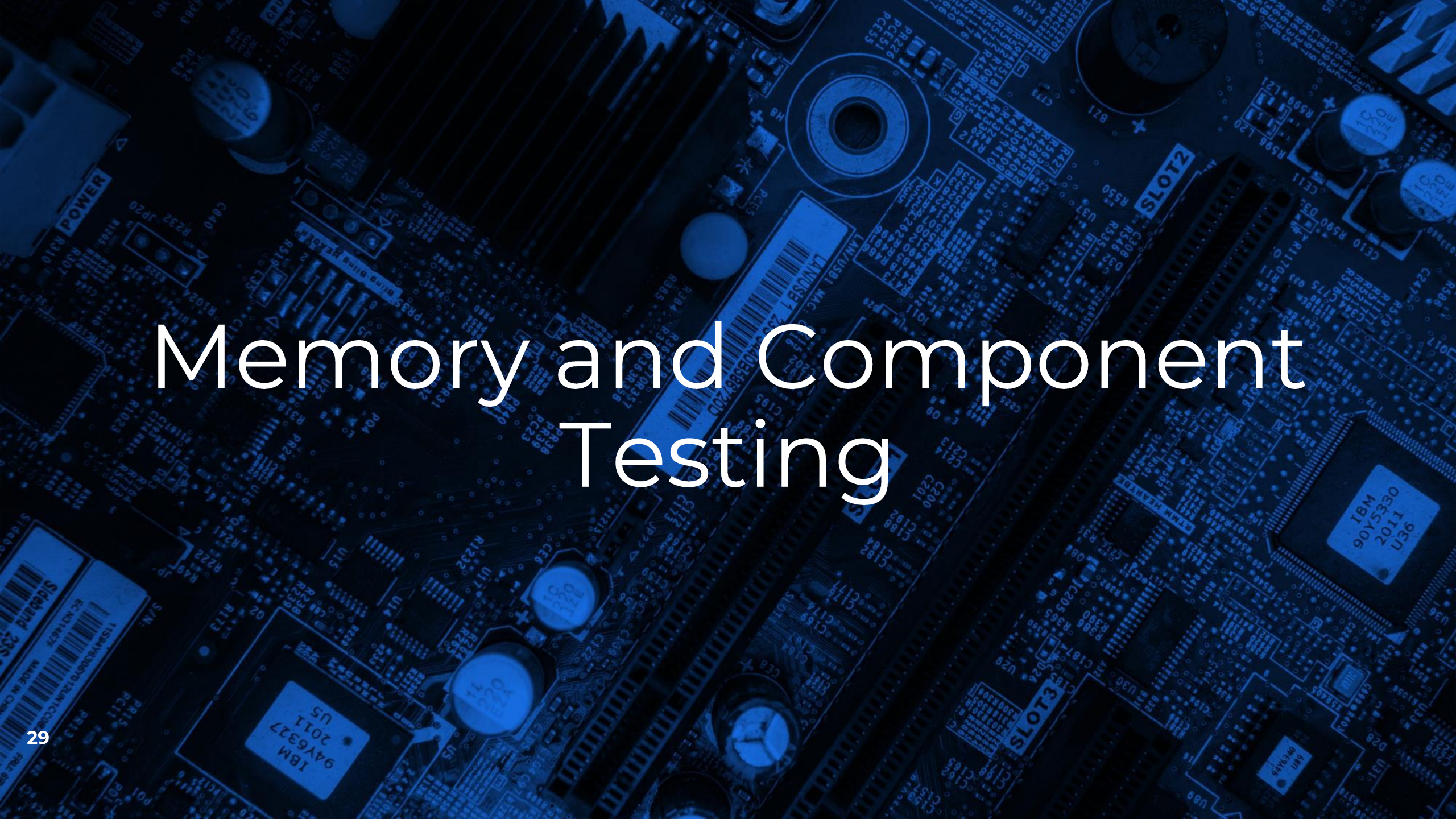


Memory and Component Testing

Memory Device Testing

PHY LEVEL TESTING

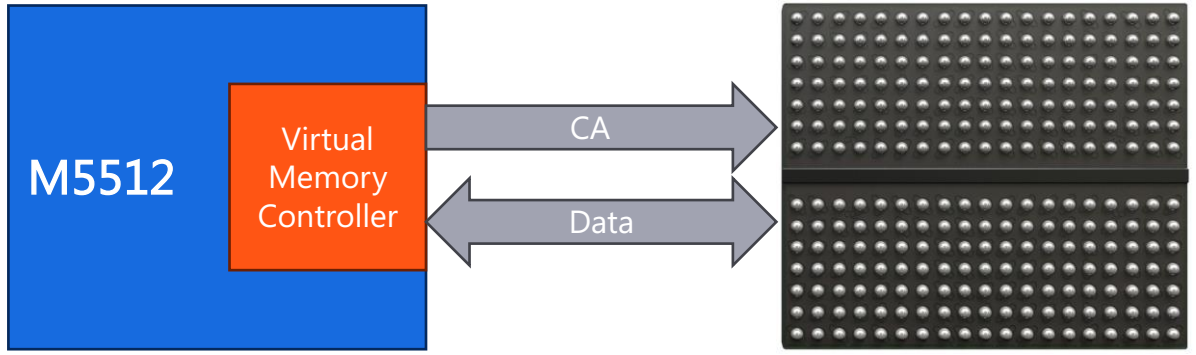
Adjustable voltage and timing parameters on all pins (including jitter injection)

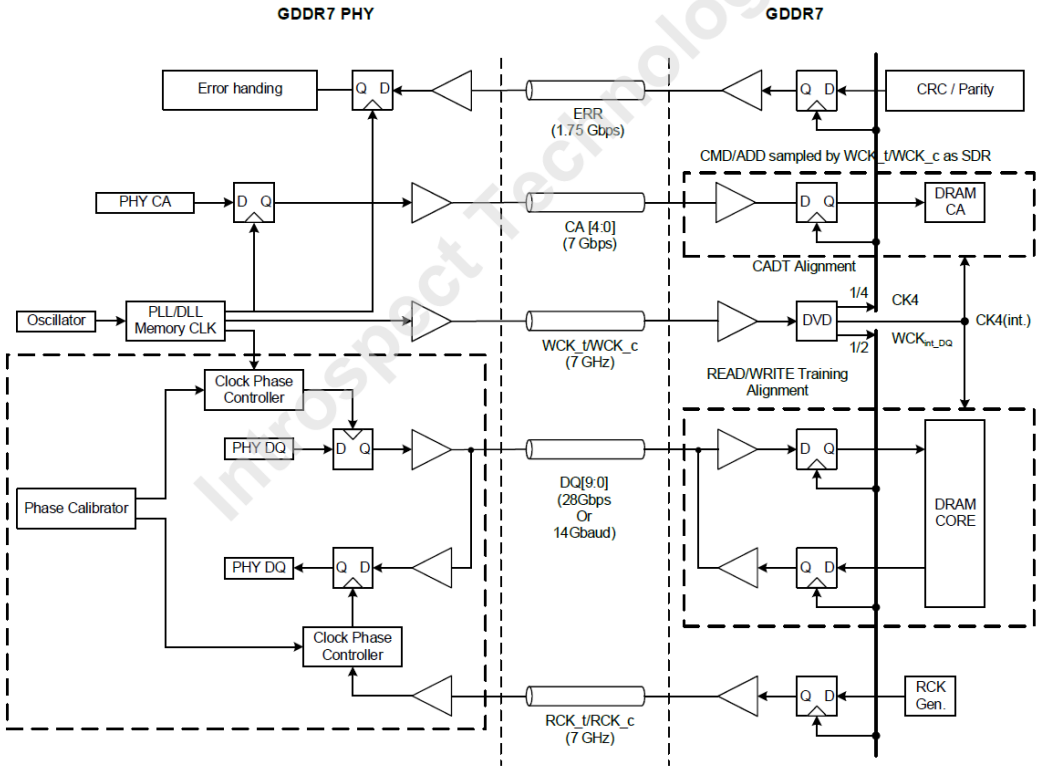
FUNCTIONAL TESTING

Protocol-compliant stimulus for all memory commands

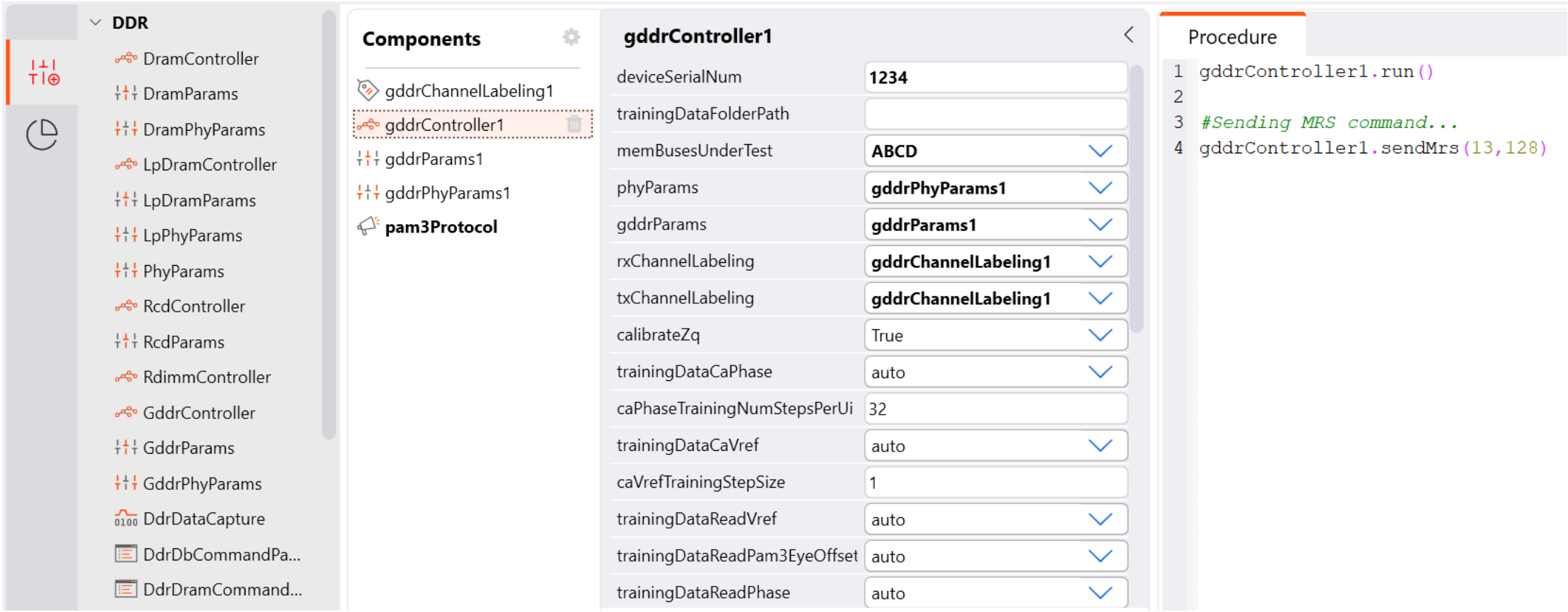
FUNCTIONAL STRESS TESTING

What are the limits of the device? Verify functional behaviour while pushing command timings, data rate and other parameters out of spec





Memory Controller Software (GD7 Example)



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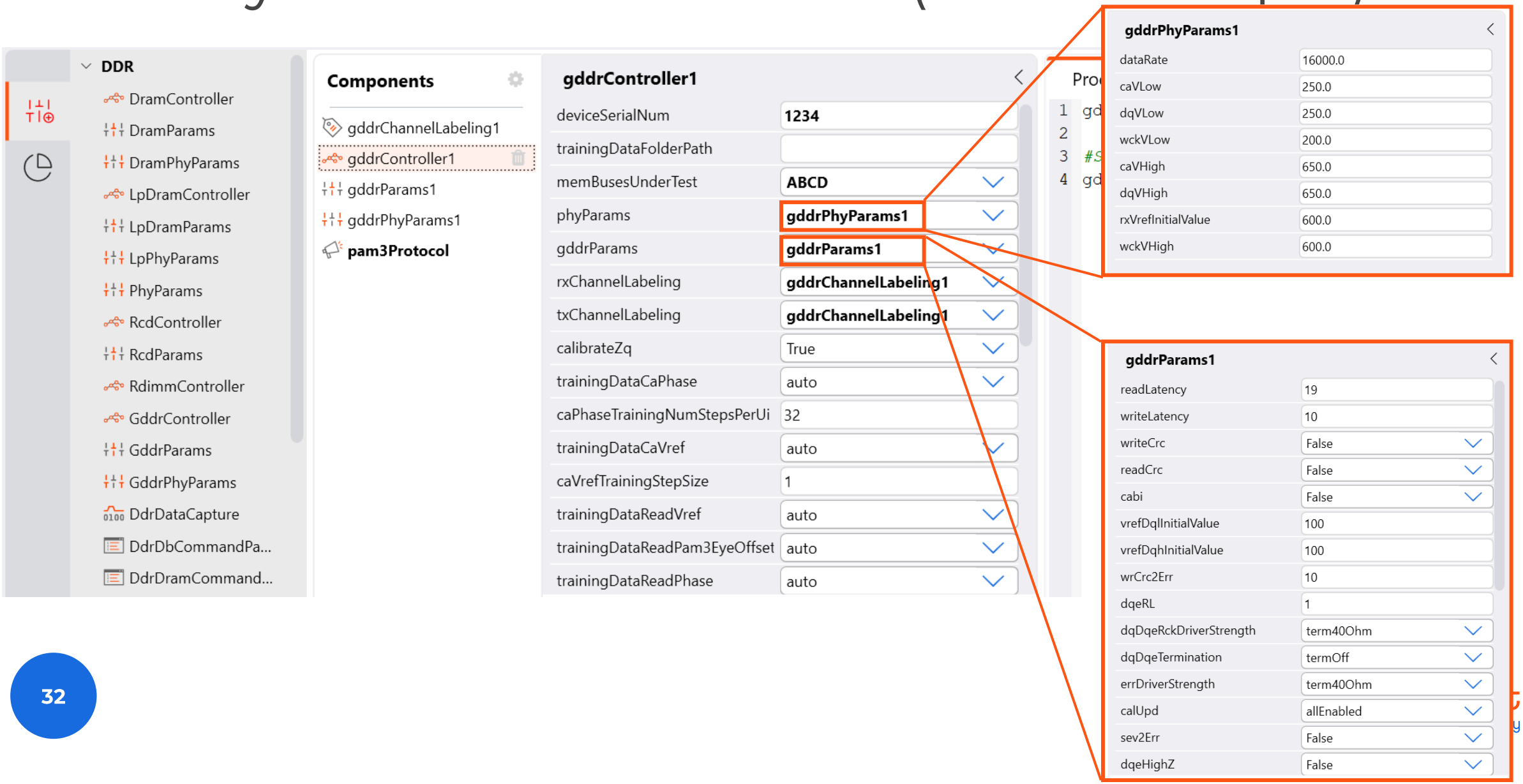
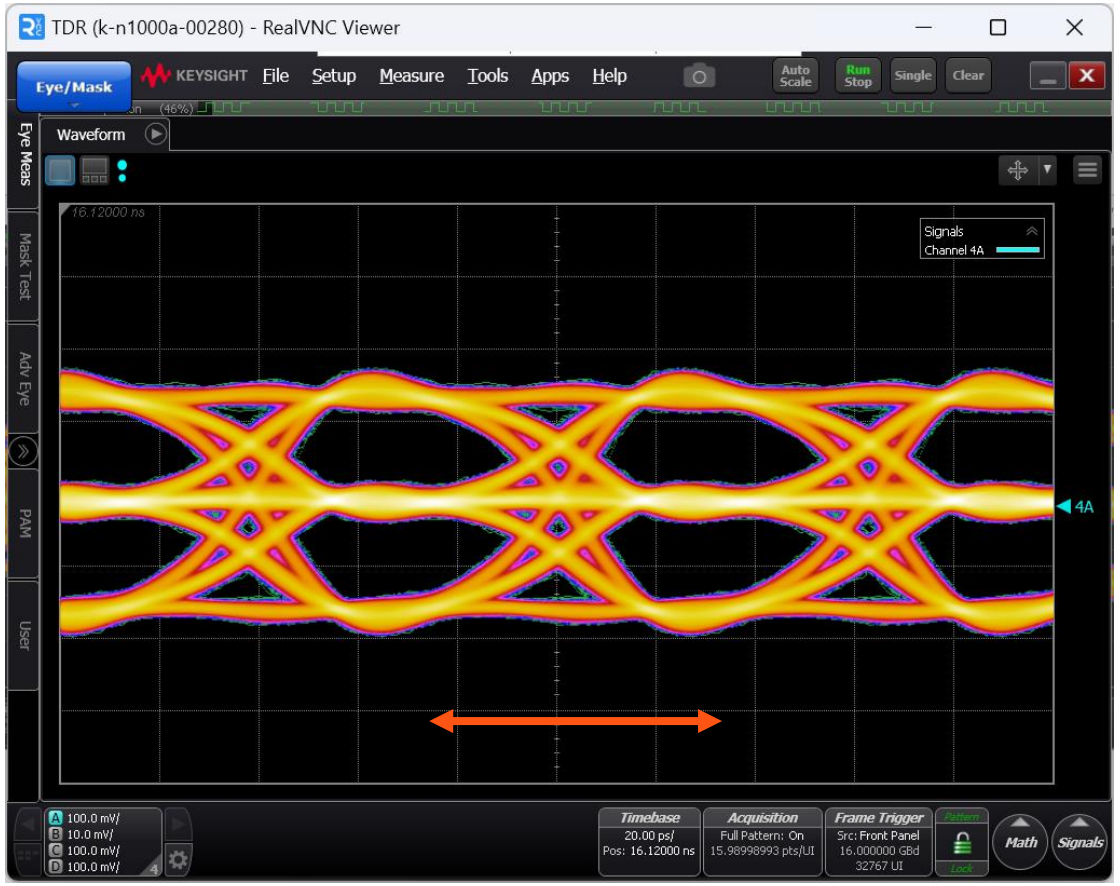
Memory Controller Software (GD7 Example)



Driver Performance – 32 Gbps



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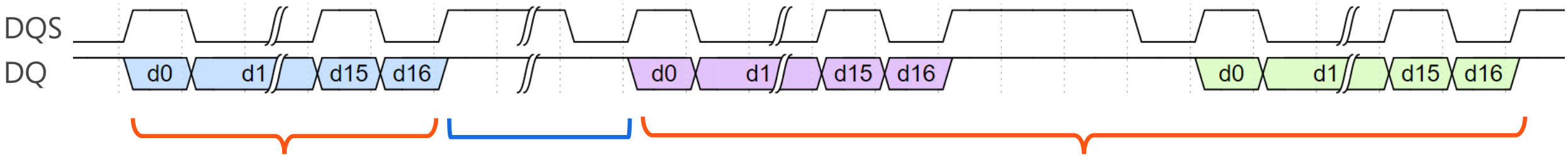
Pattern Generation Architecture

HOLD PATTERNS DRIVE IDLE STATES IN BETWEEN PATTERN SEQUENCES

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Pattern Generation Architecture

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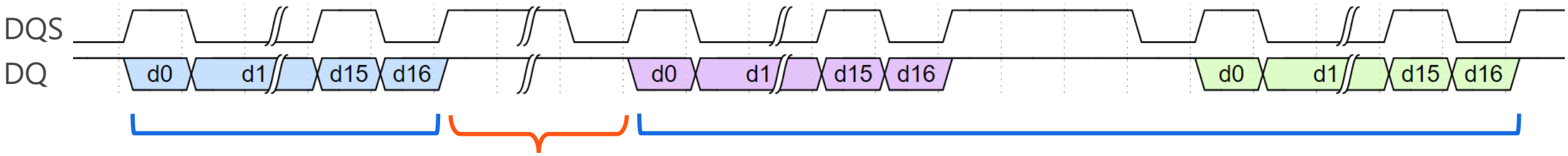

Start jitter injection on WCK…

Modify signal voltages levels on CA…

Control timings between DQ signals…

Change slew rate on DQ signals…

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Tuned Virtual Memory Controllers

DDR5 DRAM

Used to connect to a single DDR5 DRAM

Component test paradigm

RCD/MRCD

Used to connect to a single RCD or MRCD device

Component test paradigm

RDIMM/MRDIMM

Used to connect to an entire RDIMM

System-level test paradigm

LPDRAM

Used to connect to a single LPDRAM memory

Component test paradigm

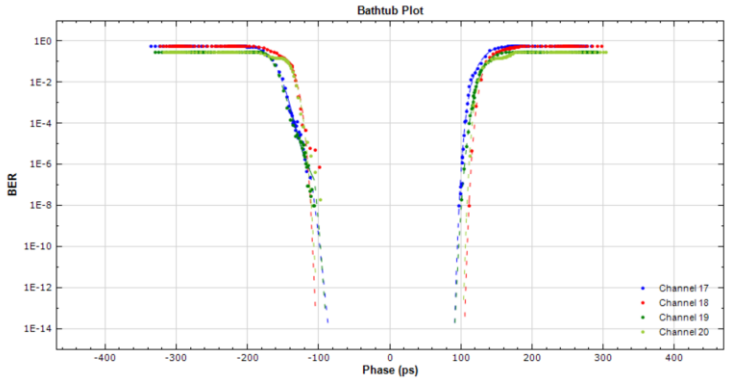
GDDR

Used to connect to a single GDDR memory

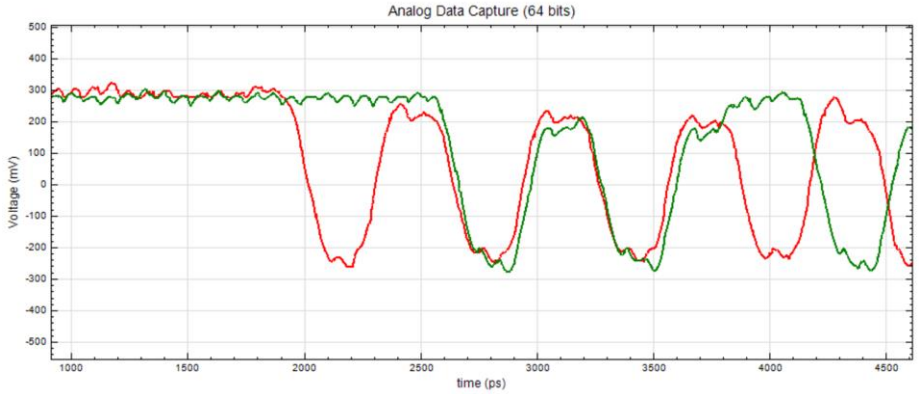
Component test paradigm

Transmitter Characterization

- Clock to data skew measurement
  - DQS to DQ
  - CK to CA
  - BCK to BCOM
- BERT measurements on clock and data
  - Long duration error rate tests
  - Eye diagrams
  - Jitter measurements
  - Slew rate measurements



DQS and DQ jitter measurement



DQ to DQS skew measurement

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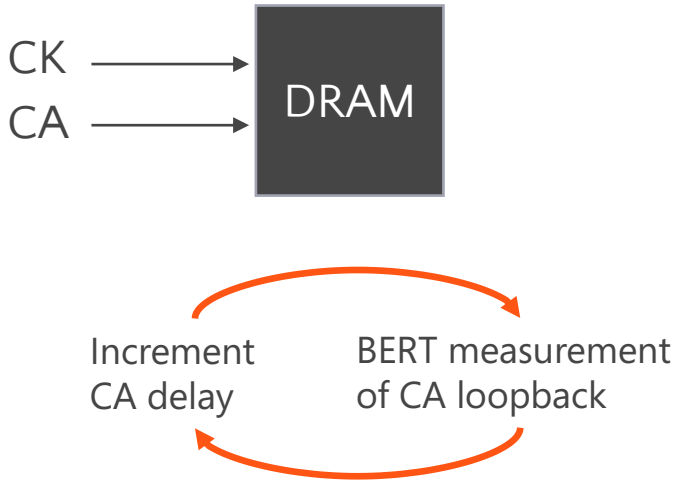
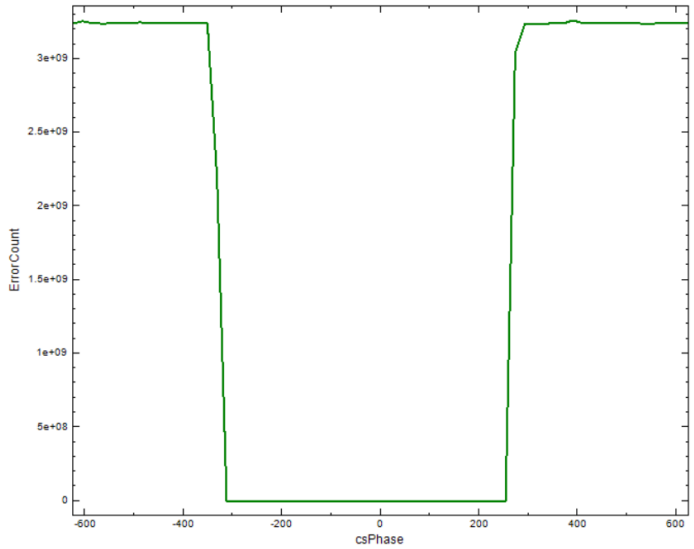
Receiver Characterization

- Requires support of different loopback/training modes or uses write and read commands
- Measure horizontal and vertical eye opening at receiver while applying different stressors
  - Jitter sensitivity – clock to data skew
  - Voltage sensitivity
  - Stressed eye





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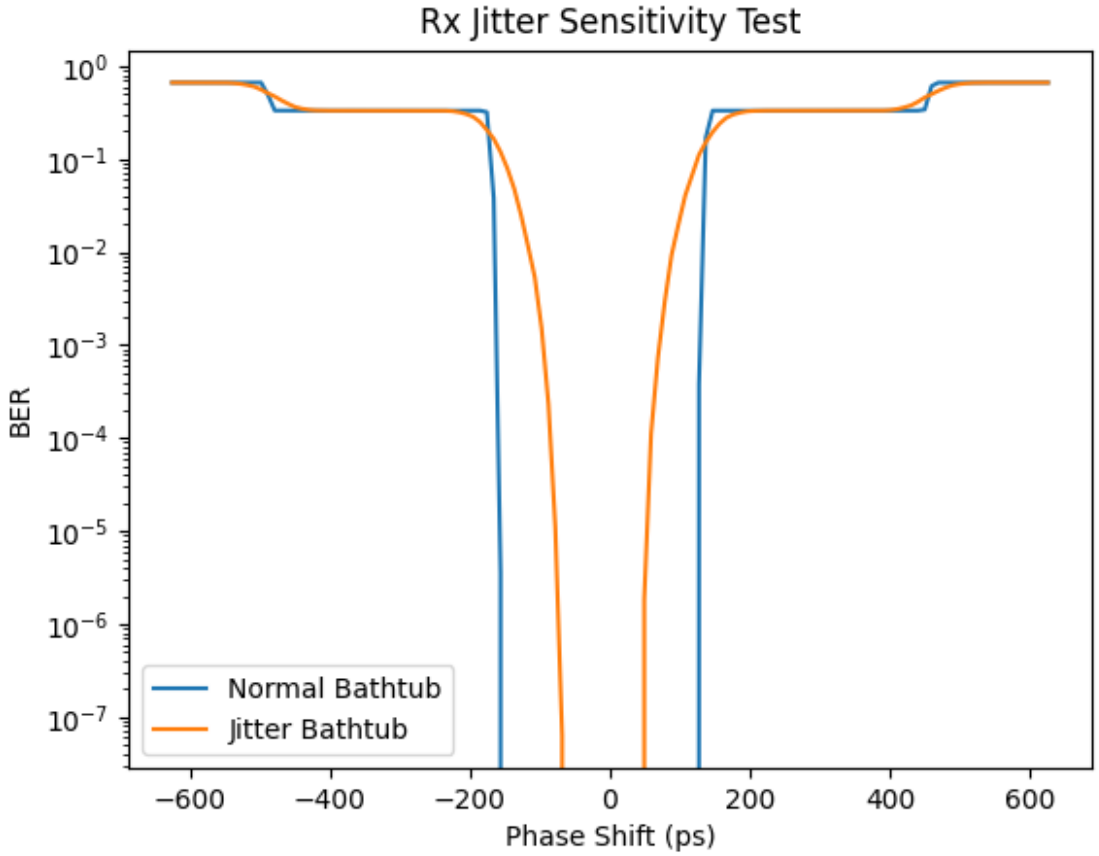
Example Receiver Stress Test Result



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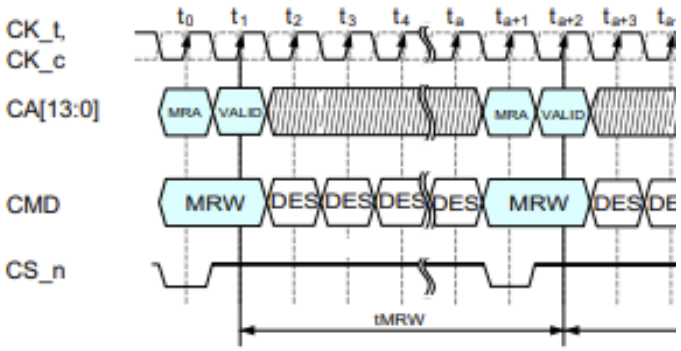
Functional Testing

- Perform pass/fail checks of device behaviour under normal test conditions
- There is a wide variety of tests in this category, that can be roughly categorized as follows
  - **Functional mode tests** – E.g. Training modes, power down, DDR/SDR operation
  - **Input spec checks** – E.g. Mode register writes, MPC commands
  - **Output spec checks** – E.g. QCS operation, output inversion, Qx output delay

MODE REGISTER WRITE TEST EXAMPLE

Send MRW commands to RCD → Read RW contents over sideband bus



PASS if read and write data match

FAIL if no match

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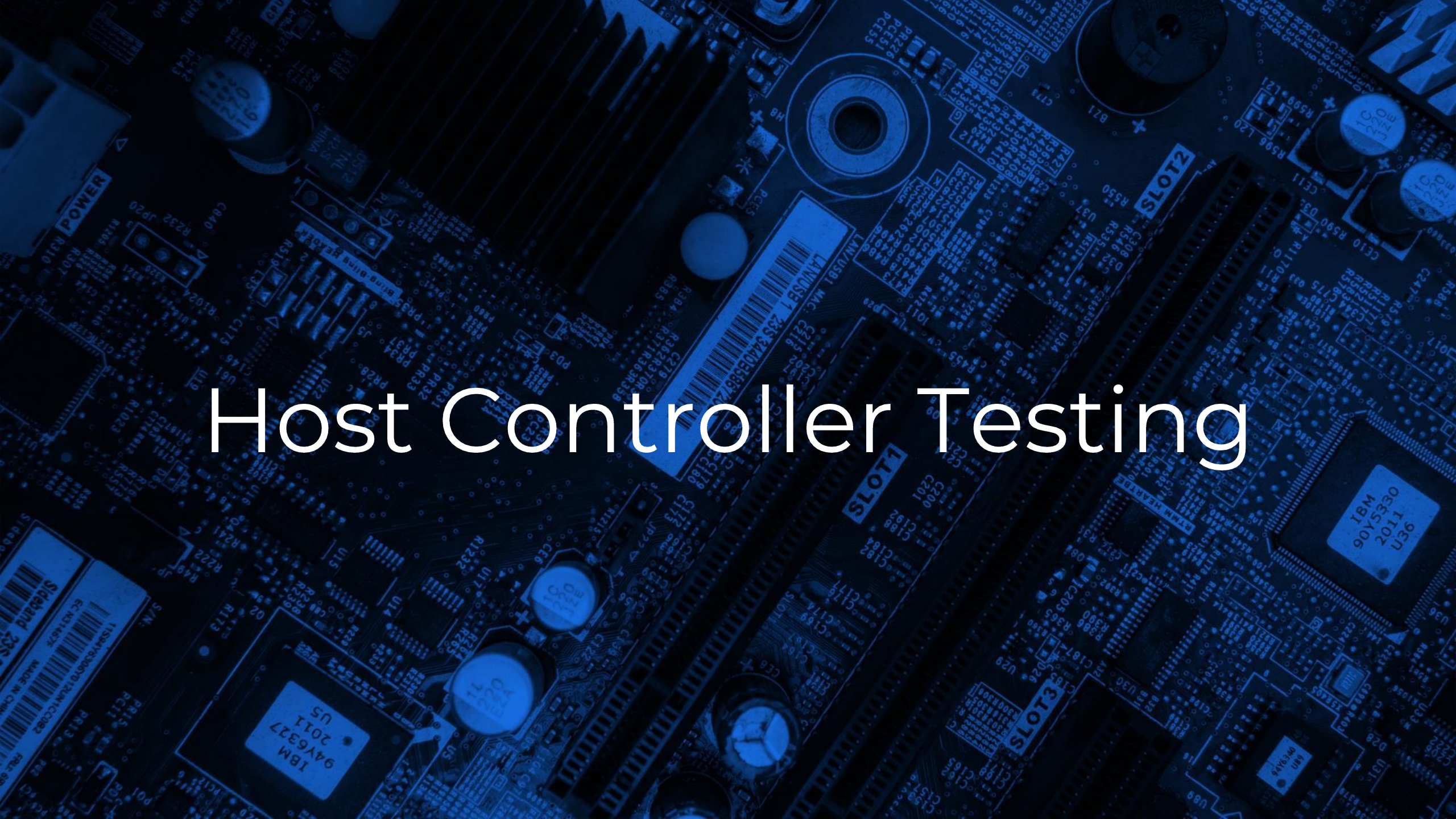
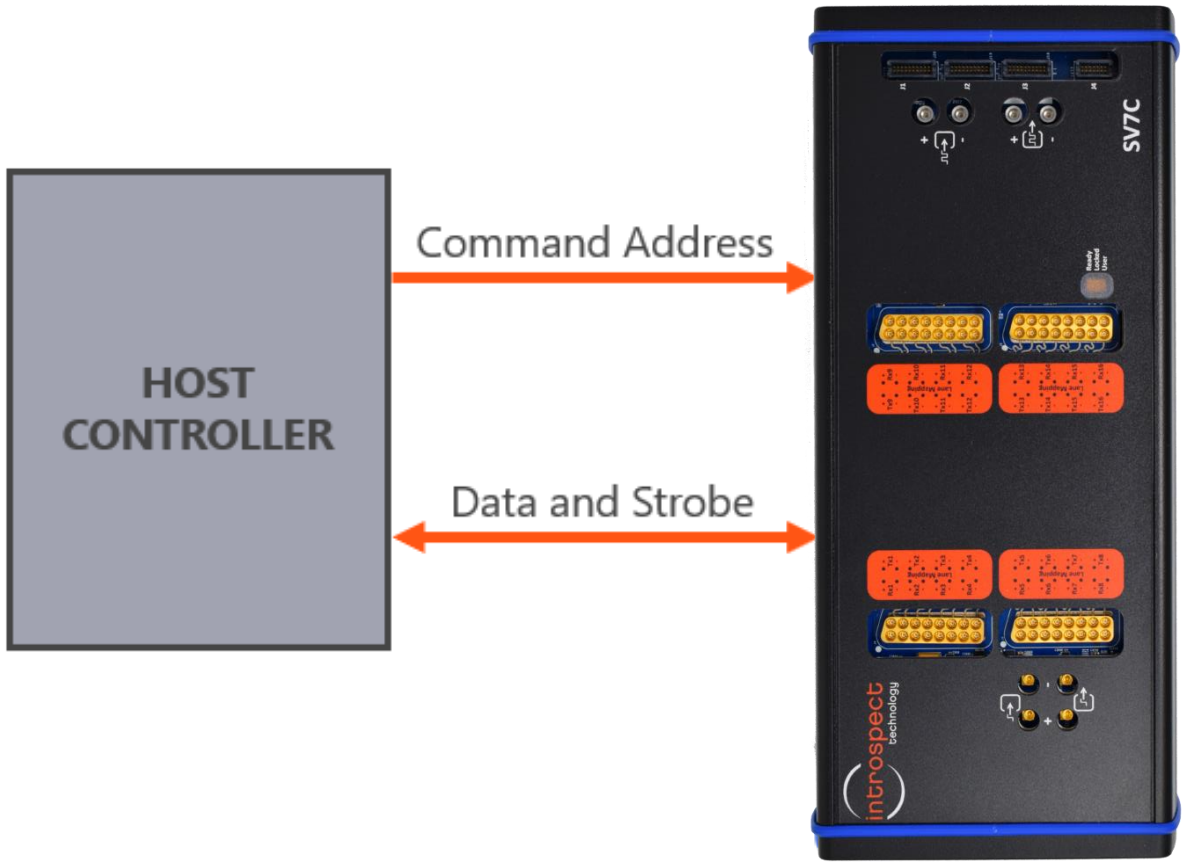

Host Controller Testing

Controller Testing

- Supports TX testing of command and data bus
  - Clock to data skew measurements
  - Eye diagrams, BER measurements etc…
- Supports RX testing of data bus using flexible pattern features and analog impairment controls. Requires loopback outputs, built-in error counters, or similar test mode in the host controller.



There is no formal JEDEC spec for the memory controller, so test conditions and pass/fail requirements are not defined.

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Pattern Generation

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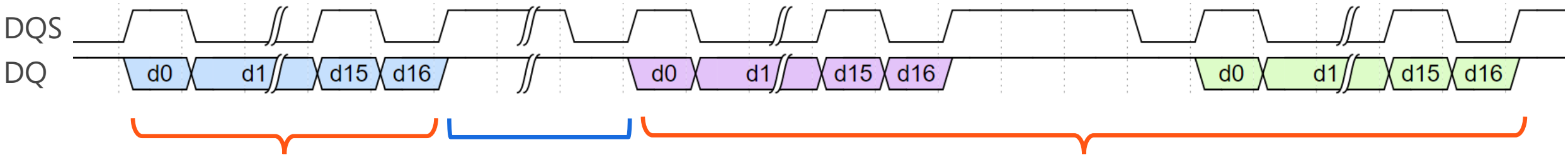


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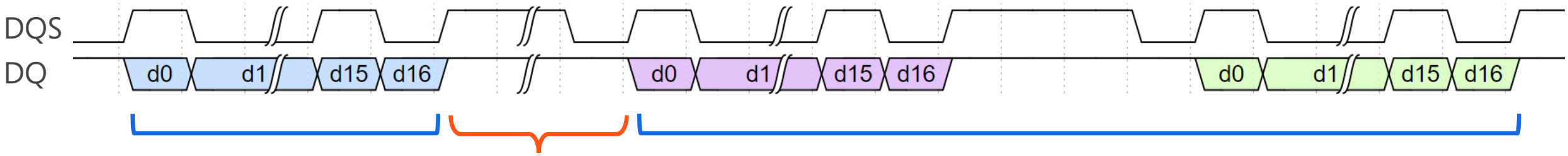

Start jitter injection

Modify signal voltages levels

Control timings between signals

Change slew rate

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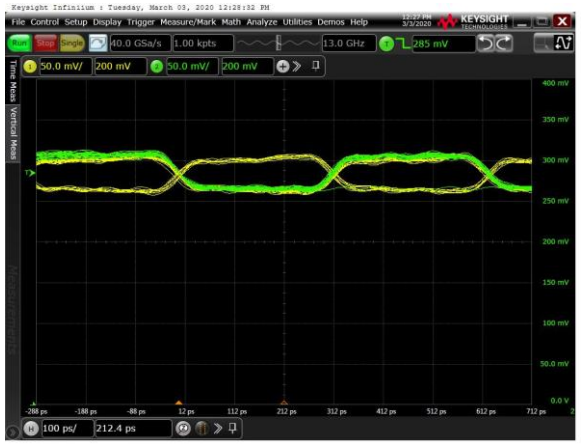
Timing and Voltage Control

PER LANE PHASE, AMPLITUDE AND COMMON MODE SETTINGS



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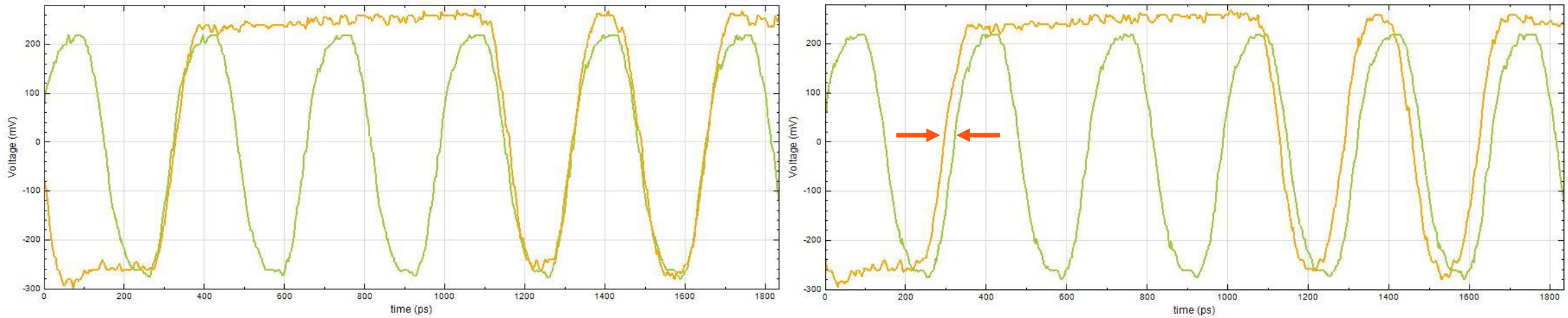
Transmitter Skew Measurement

MEASURE CHANNEL TO CHANNEL SKEW

Detect and measure DQ to DQS delay



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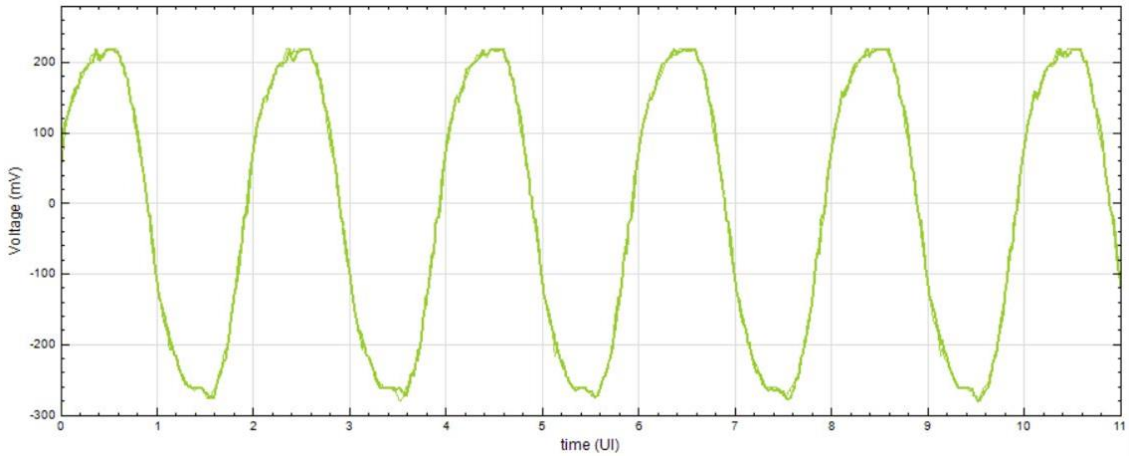
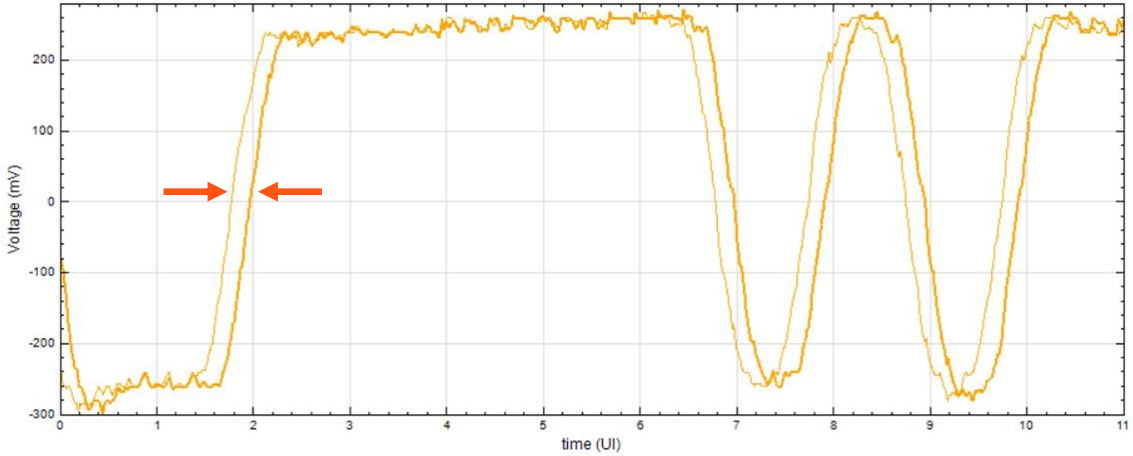
Transmitter Skew Measurement

VIEW PATTERN ALIGNMENT ON A SINGLE CHANNEL OVER TIME

DQS position is constant



DQ position has changed



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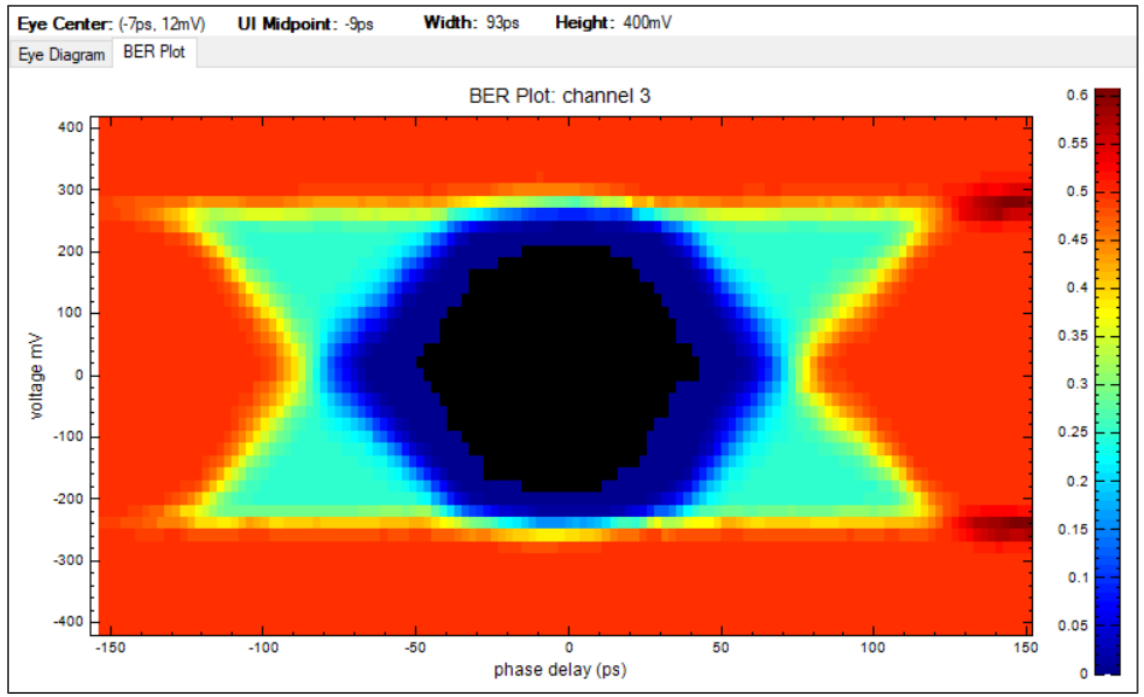
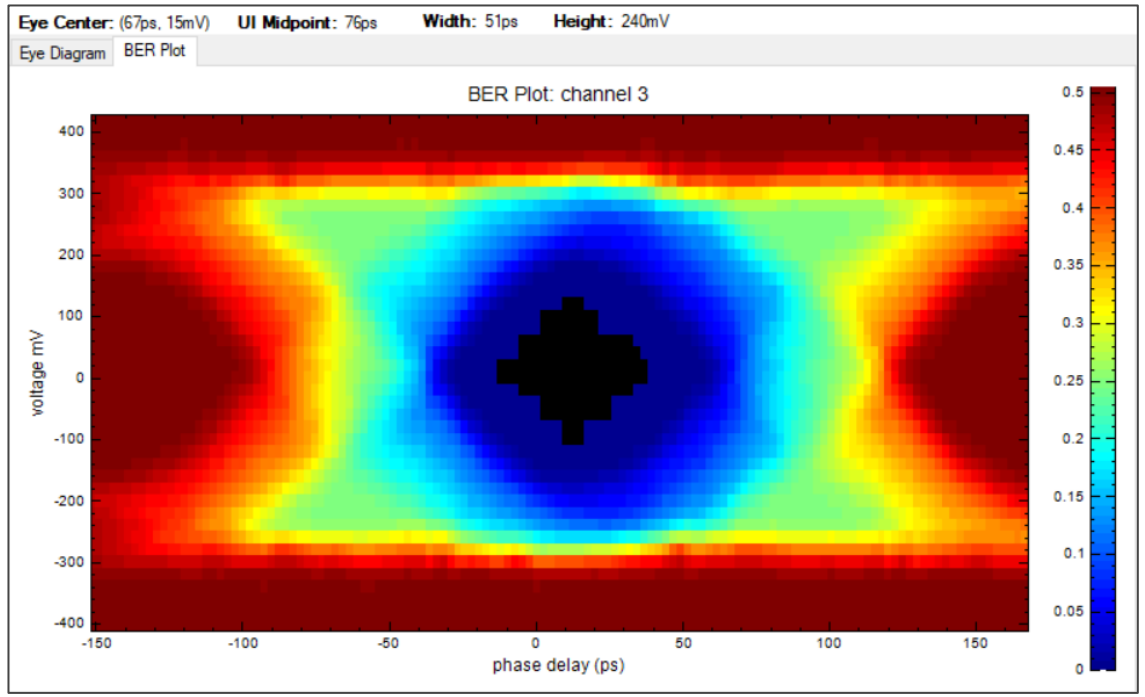
BERT Measurements





Eye diagrams across different transmitter slew rate settings

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Burst Mode Digital Capture

CAPTURE AND FILTER OUT BURST DATA

DQS

DQ0

Bits | Analysis | Bursts

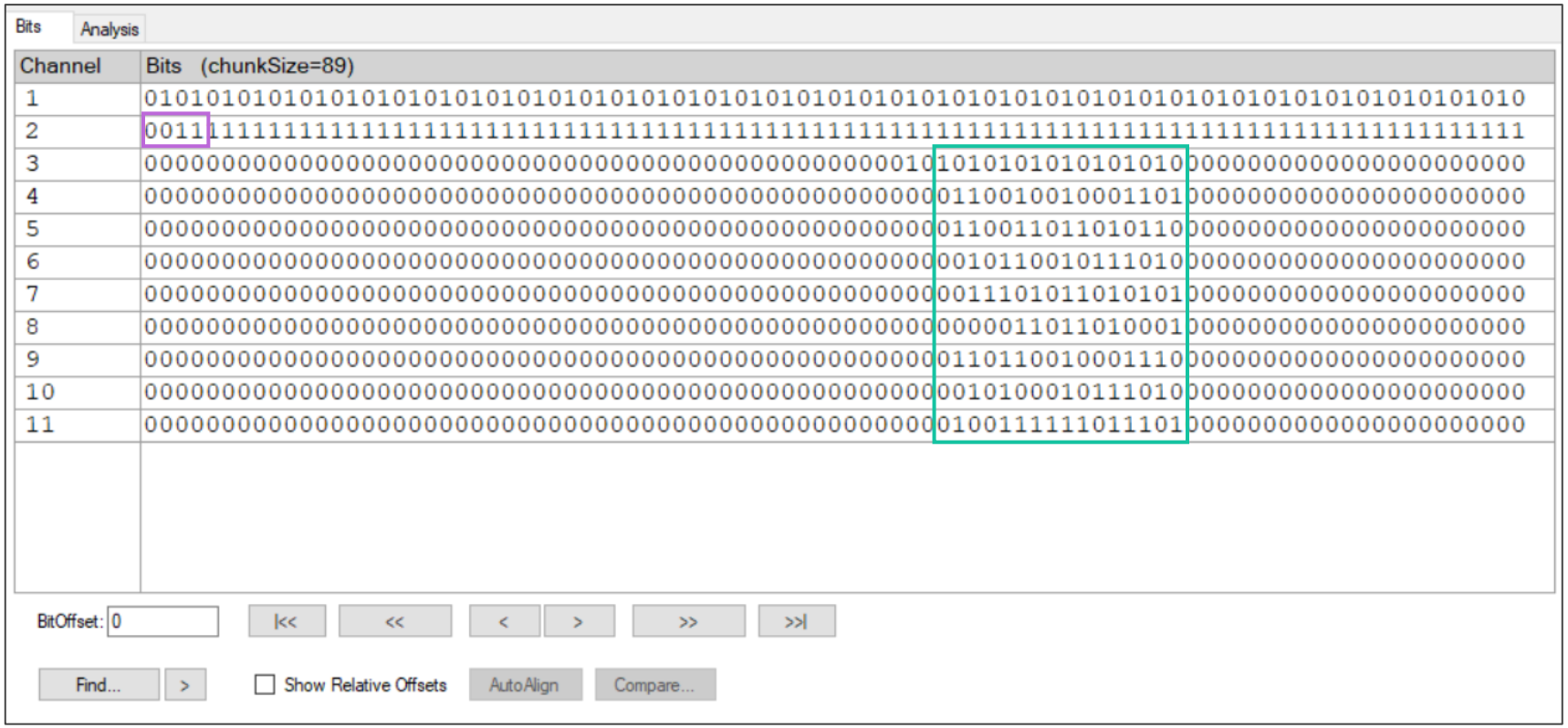
Channel	Burst#	Offset	Status	Bits
1				
	0	2	good	1010101010101010
	1	66	good	1010101010101010
	2	130	good	1010101010101010
	3	194	good	1010101010101010
	4	258	good	1010101010101010
2				
	0	2	good	0111011000110000
	1	66	good	0101000010100100
	2	130	good	0011001010110100
	3	194	good	0111011000110000
	4	258	good	0101000010100100

Triggered Digital Capture

ONE-SHOT TRIGGER ON COMMAND AND CAPTURE DATA BUS IN PARALLEL

CK
CS

Data
Bus



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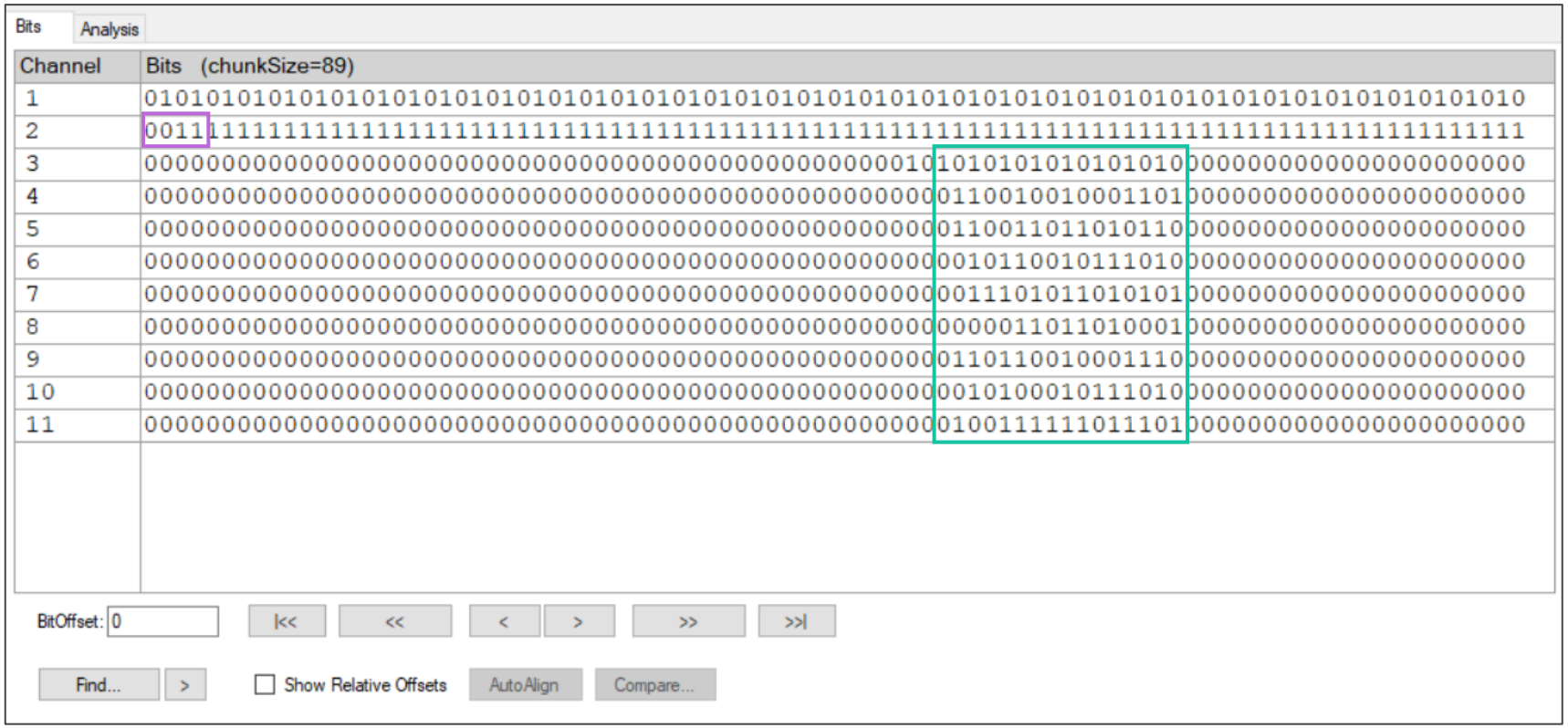
Continuously Triggered Capture

KEEP TRIGGERING ON COMMANDS (PROTOCOL ANALYZER)

CK
CS

Data
Bus



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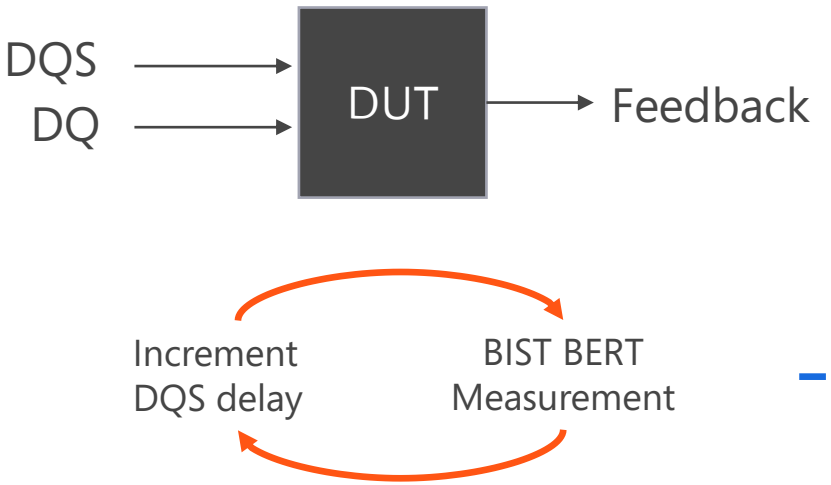
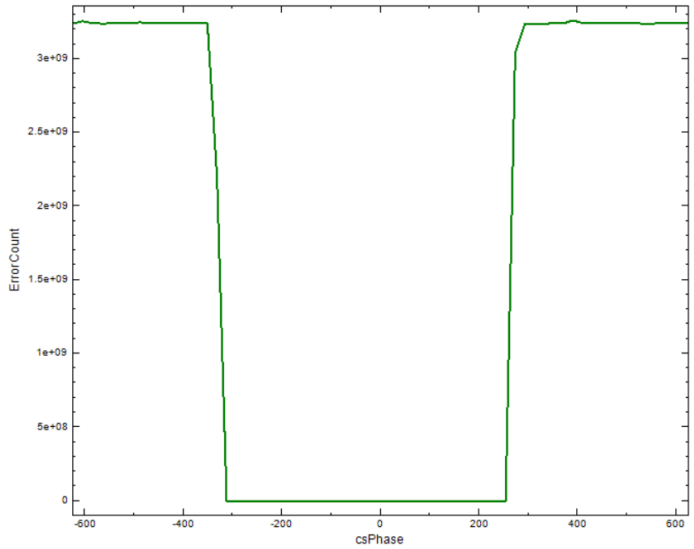
Receiver Characterization

- Requires support of checking errors within the memory controller component
- Measure horizontal and vertical eye opening at receiver while applying different stressors
  - Jitter sensitivity – clock to data skew
  - Voltage sensitivity
  - Stressed eye





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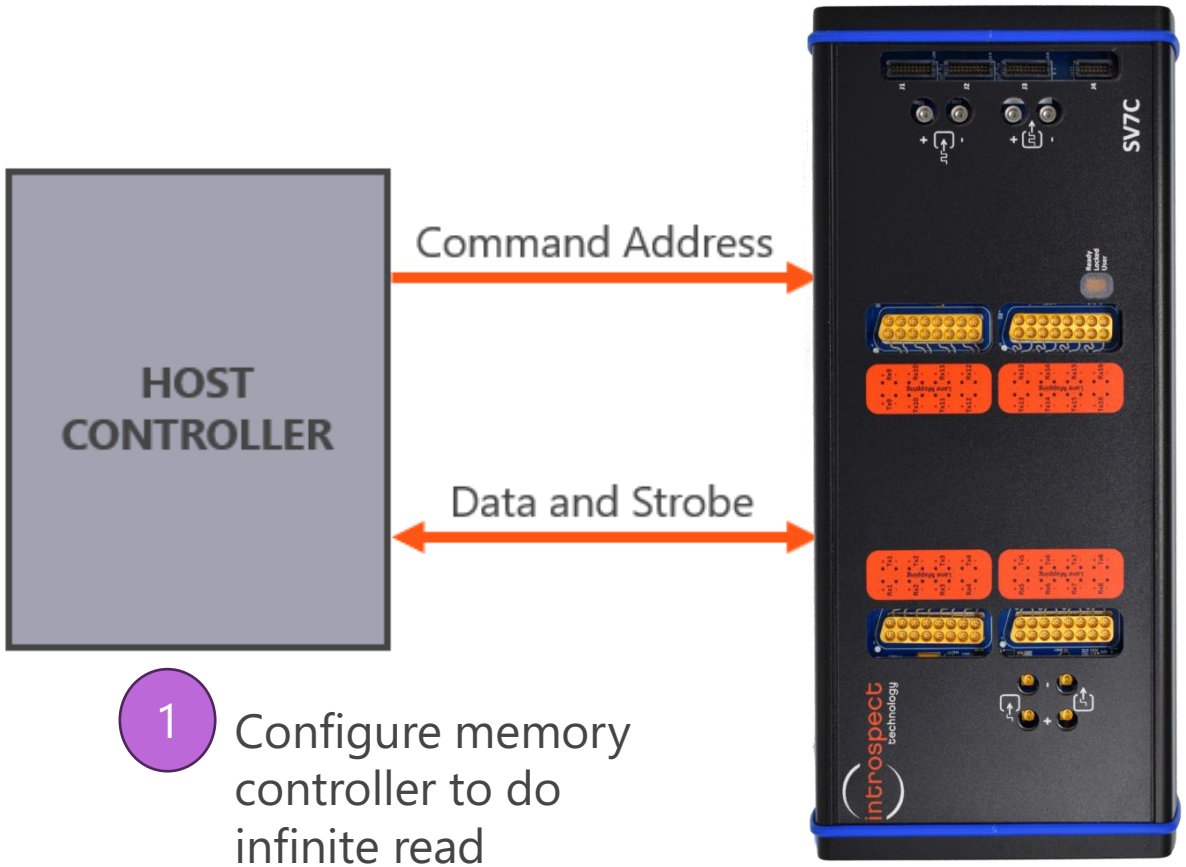
Receiver Characterization Using BIST



- Two-step receiver characterization based on memory controller BIST mode
- In the first step, the BIST is enabled to perform infinite write/read operations or infinite read operations
- In the second step, the SV7C is programmed in Python to prepare the read response data and then transmit it

1 Configure memory controller to do infinite read operation with BIST checker

2 Pre-program read responses and read timings inside SV7C-17 and send the data with impairments

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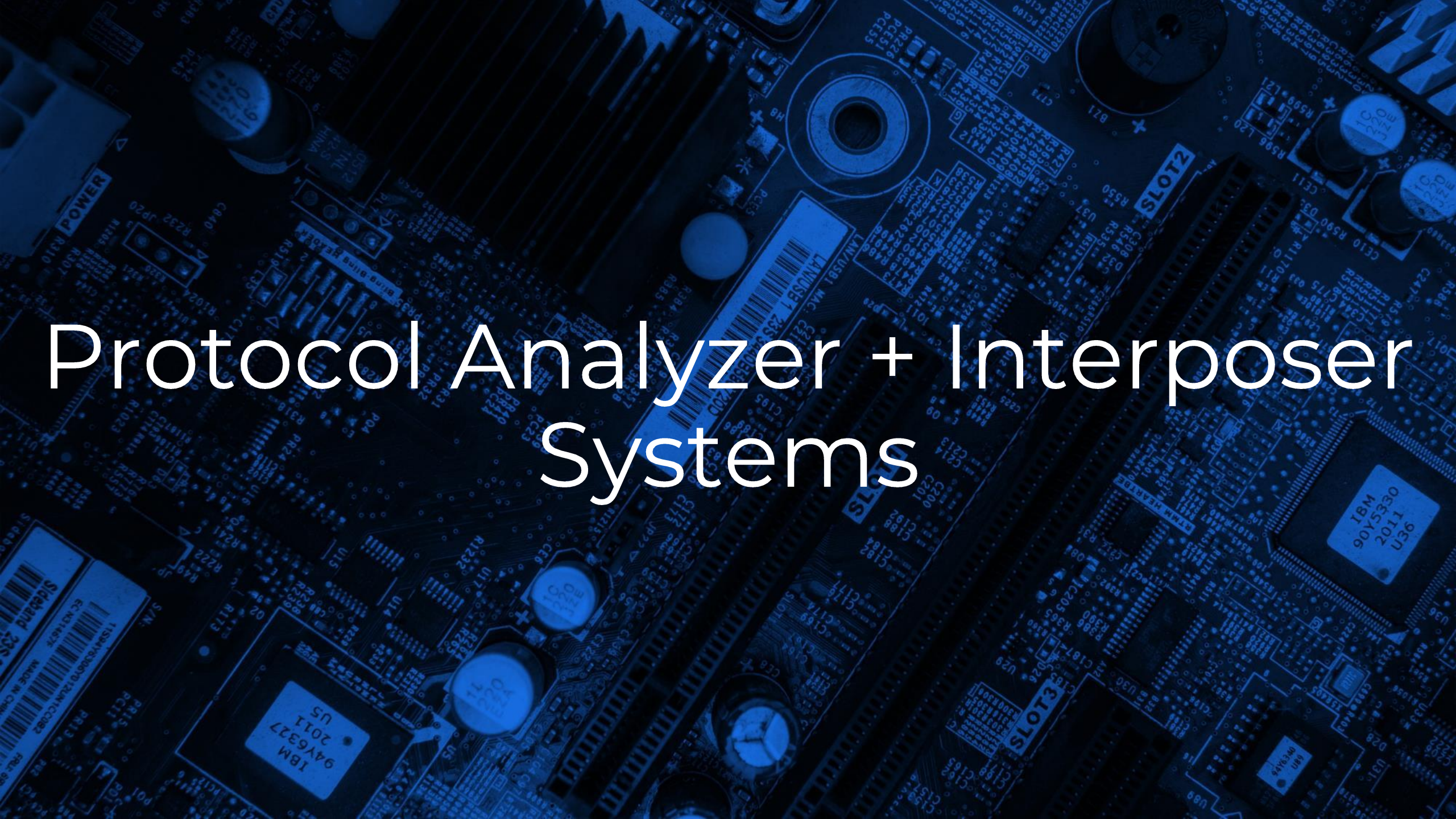
Protocol Analyzer + Interposer Systems

DDR5/LPDDR5 Protocol Analyzer

ANALYZER INSTRUMENT

Same exerciser hardware but with a license for protocol analyzer

Remote Sampling Heads (Up to 32 Channels)

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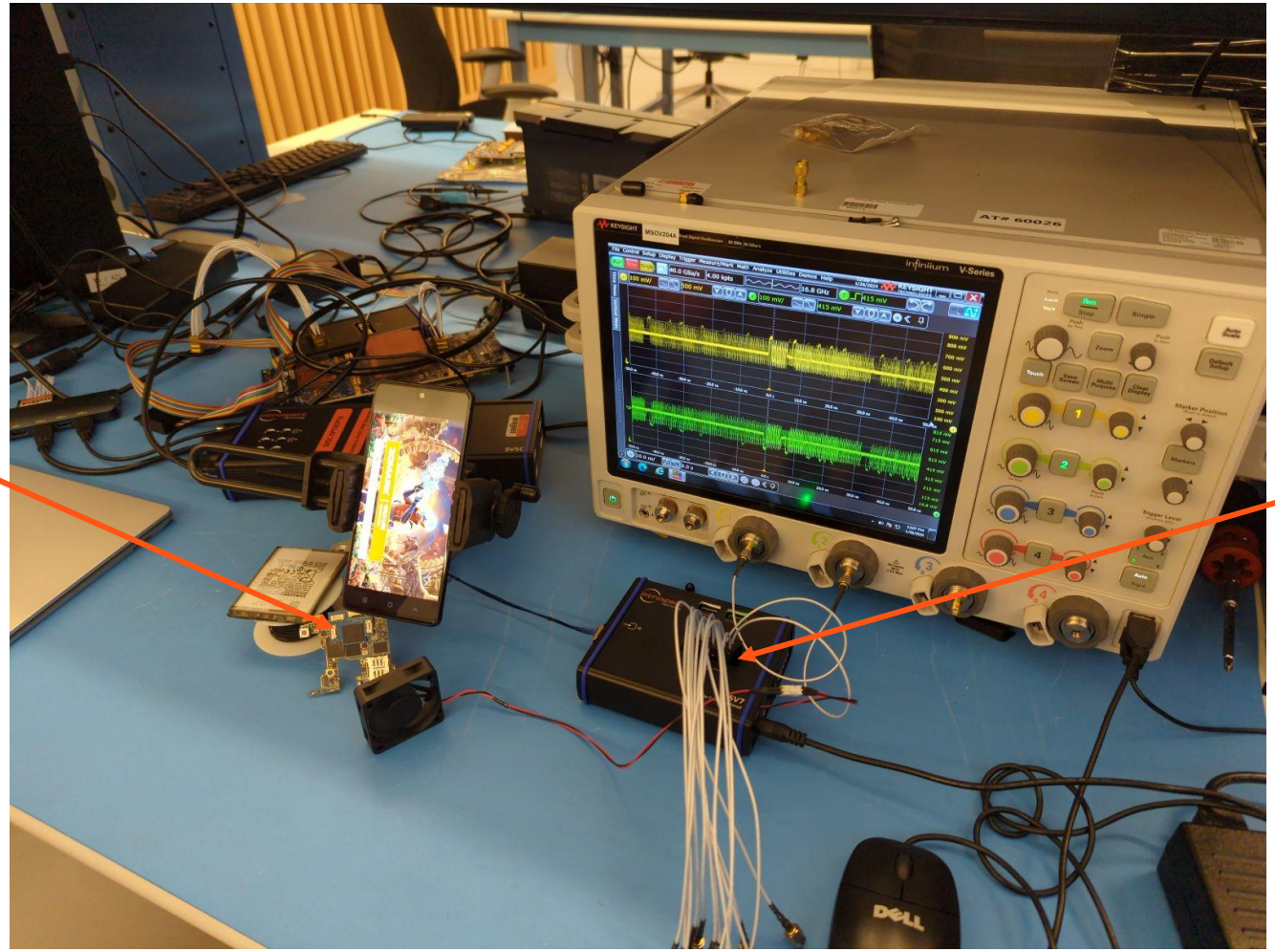
DDR5/LPDDR5 Protocol Analyzer

INTERPOSER SYSTEM

Interposer system (example shown is PoP LPDDR5)



Remote Sampling Head (multi-channel active probe) connected to oscilloscope

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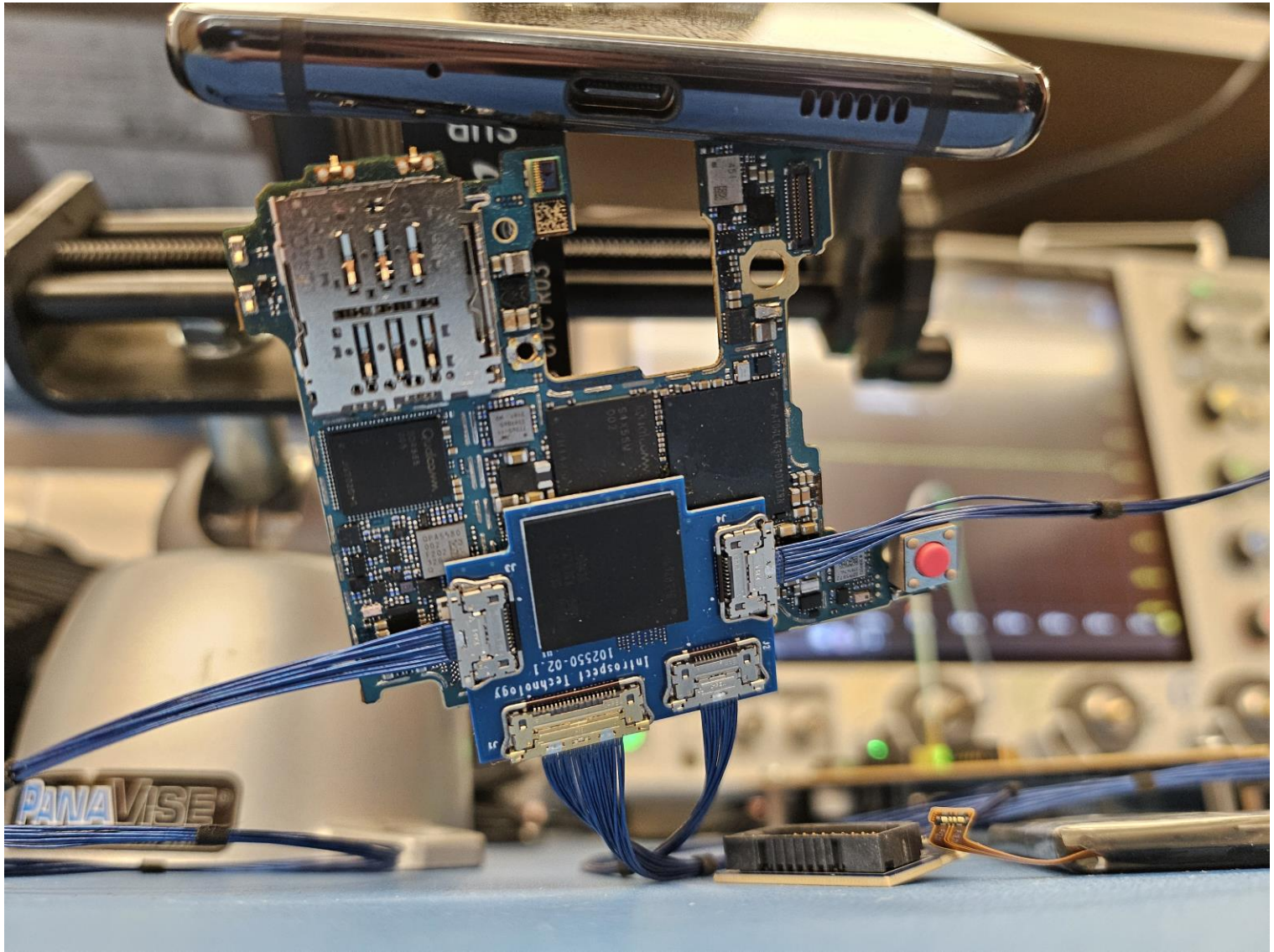
Zoomed View With All Pins Probed



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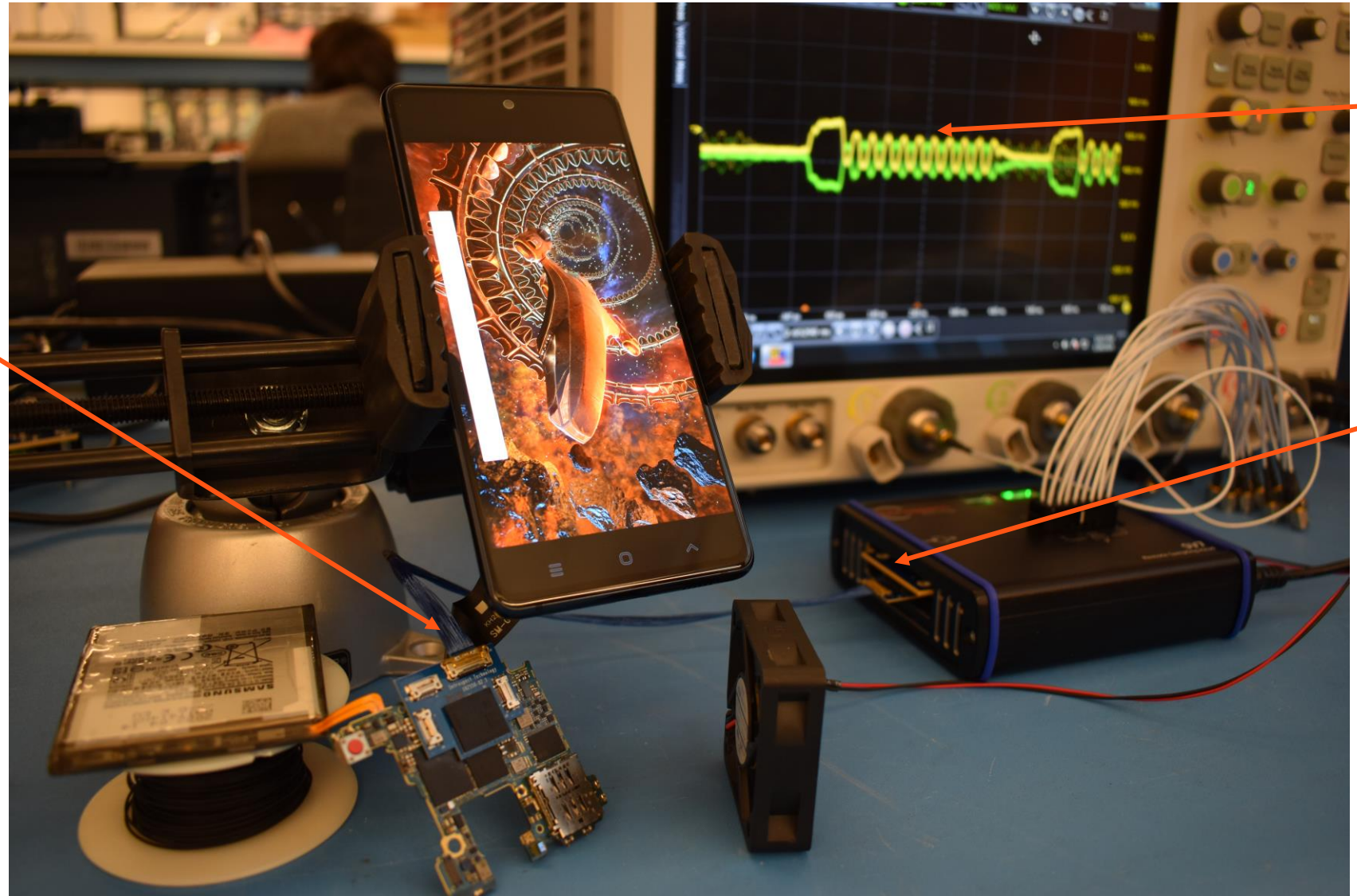
Probed Waveform Visible on Scope



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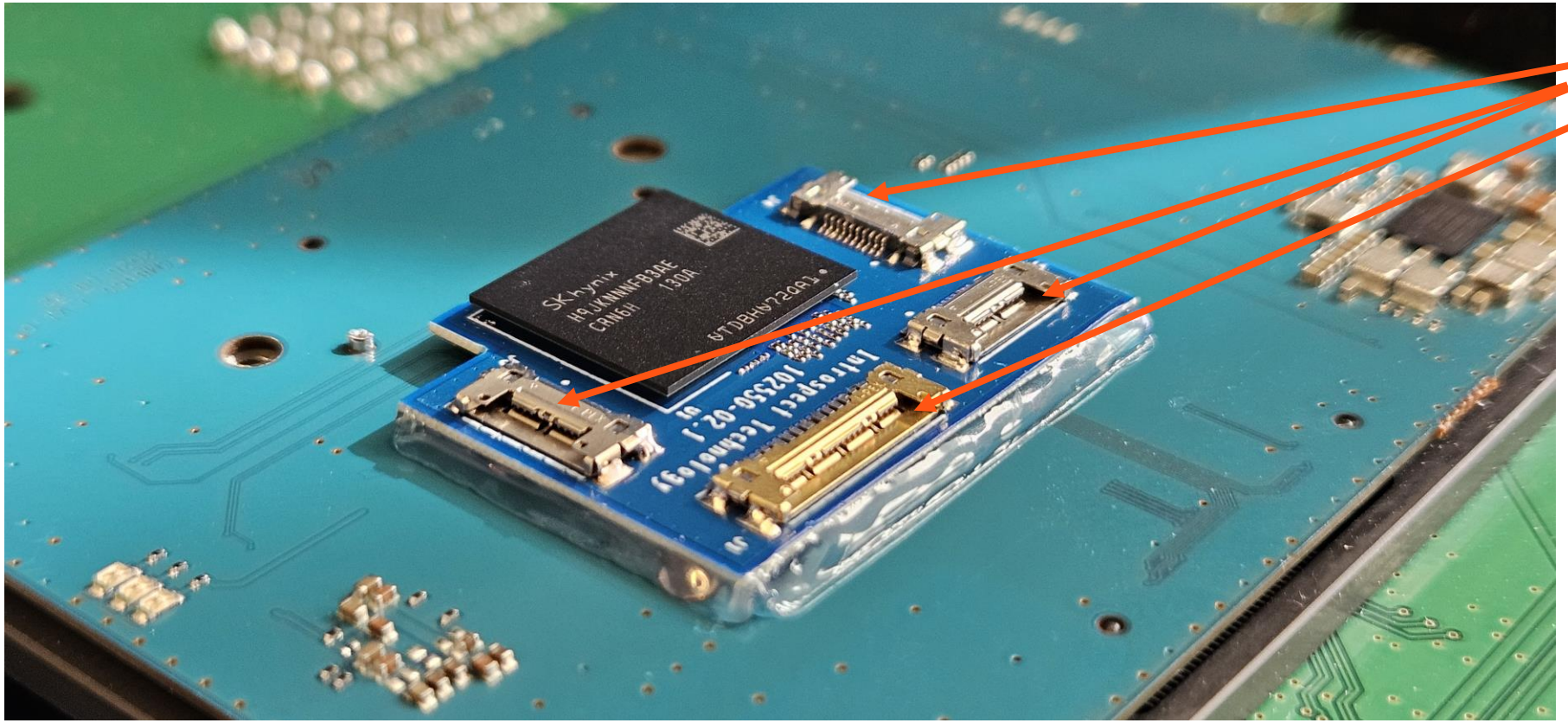
Example Evaluation Board



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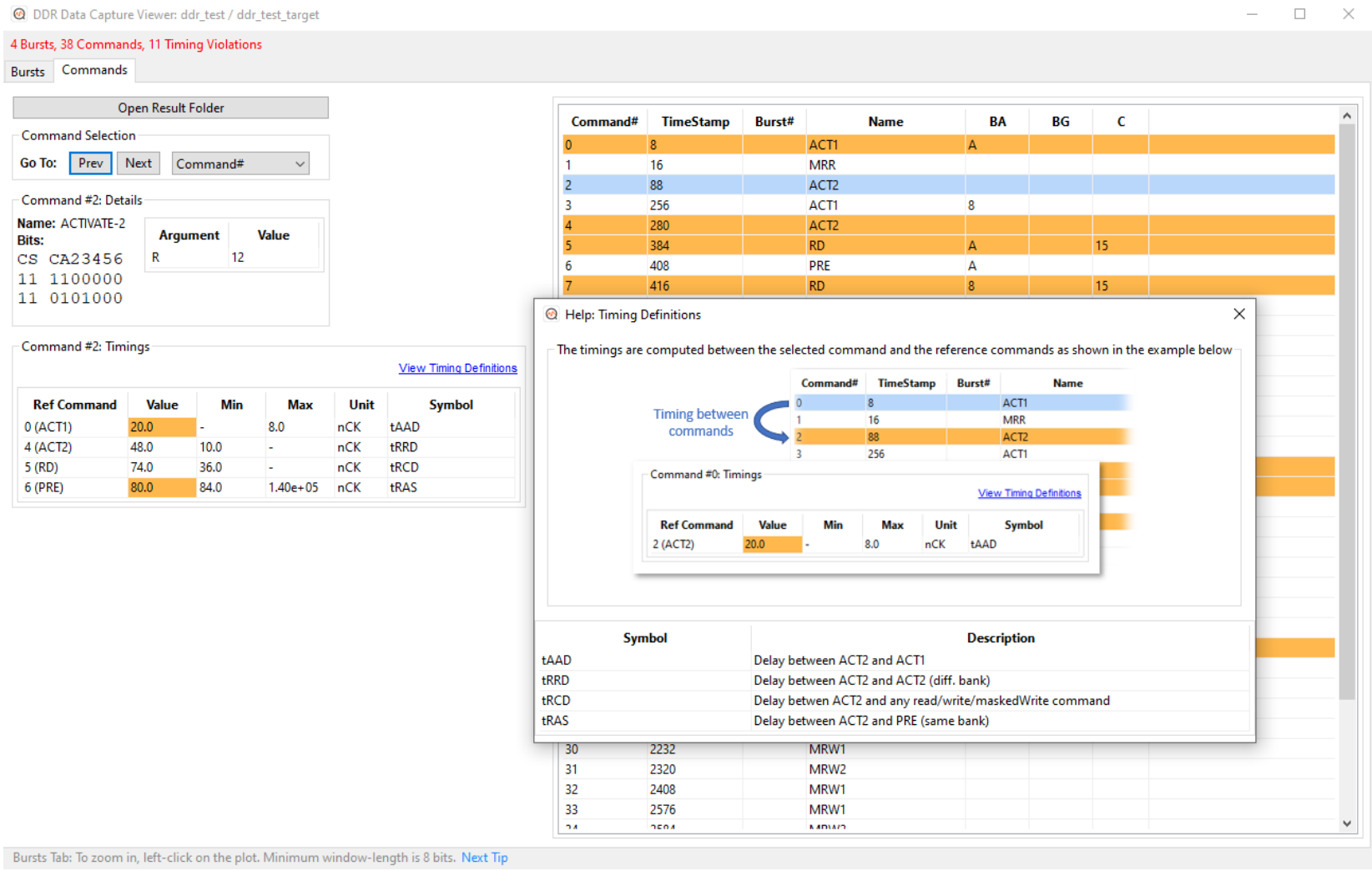
DDR5/LPDDR5 Protocol Analyzer

FULL PROTOCOL ANALYSIS



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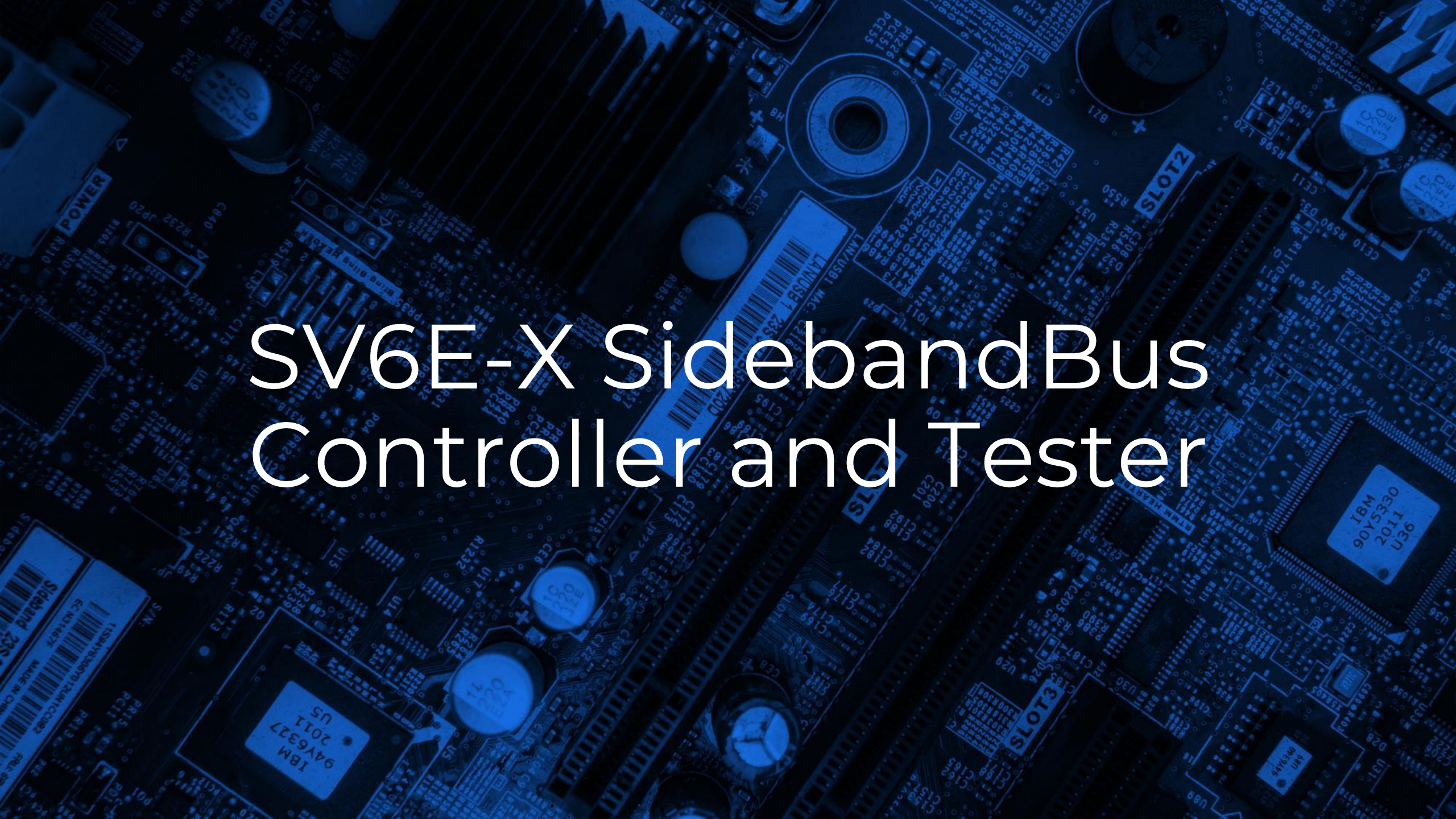
SV6E-X SidebandBus
Controller and Tester

E SERIES

SV6E-X – I3C License

Mid-Frequency Digital Test Module

OVERVIEW

Multi-Purpose Protocol Exerciser, Protocol analyzer, real-time oscilloscope

Can be licensed for different mid-frequency digital protocols (I3C shown here)

FEATURES

- Two banks of 10 channels each
- 200 MHz operating frequency
- Two programmable, high-current power supplies
- PurVue Analyzer™ technology on any channel

BENEFITS

- Supports I3C, I3C Basic, JESD403, RCD, PMIC, SPD Hub, DMTF, MCTP
- Enables high-performance testing compared to other solutions
- Replaces racks of bench equipment or PXI test systems

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Detailed Protocol Analyzer View

Capture summary

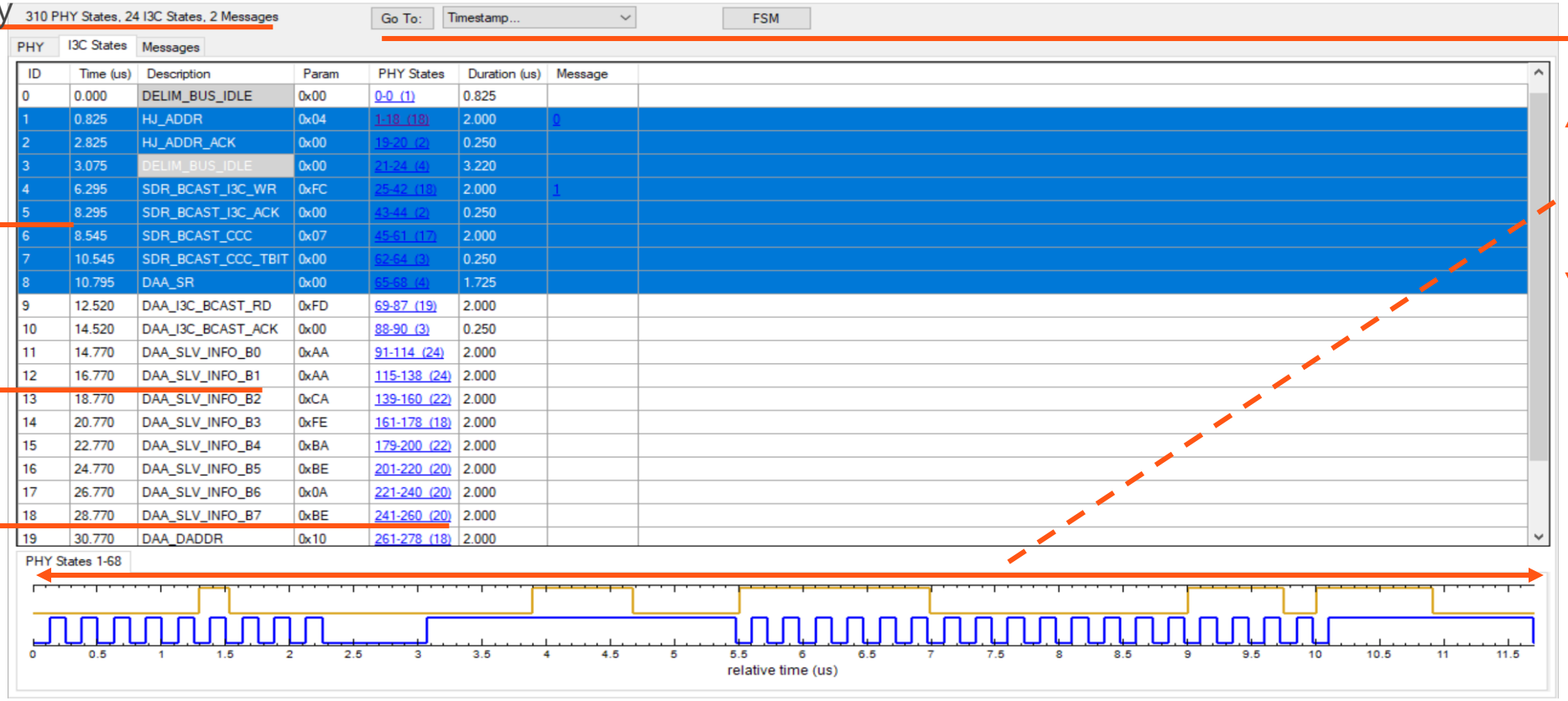
Powerful search

Precision time stamps

Human-readable event lists

Hyperlinks to toggle views

Dynamically adjust timing diagram span based on selected events



ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
0	0.000	DELIM_BUS_IDLE	0x00	0-0 (1)	0.825	
1	0.825	HJ_ADDR	0x04	1-18 (18)	2.000	0
2	2.825	HJ_ADDR_ACK	0x00	19-20 (2)	0.250	
3	3.075	DELIM_BUS_IDLE	0x00	21-24 (4)	3.220	
4	6.295	SDR_BCAST_I3C_WR	0xFC	25-42 (18)	2.000	1
5	8.295	SDR_BCAST_I3C_ACK	0x00	43-44 (2)	0.250	
6	8.545	SDR_BCAST_CCC	0x07	45-61 (17)	2.000	
7	10.545	SDR_BCAST_CCC_TBIT	0x00	62-64 (3)	0.250	
8	10.795	DAA_SR	0x00	65-68 (4)	1.725	
9	12.520	DAA_I3C_BCAST_RD	0xFD	69-87 (19)	2.000	
10	14.520	DAA_I3C_BCAST_ACK	0x00	88-90 (3)	0.250	
11	14.770	DAA_SLV_INFO_B0	0xAA	91-114 (24)	2.000	
12	16.770	DAA_SLV_INFO_B1	0xAA	115-138 (24)	2.000	
13	18.770	DAA_SLV_INFO_B2	0xCA	139-160 (22)	2.000	
14	20.770	DAA_SLV_INFO_B3	0xFE	161-178 (18)	2.000	
15	22.770	DAA_SLV_INFO_B4	0xBA	179-200 (22)	2.000	
16	24.770	DAA_SLV_INFO_B5	0xBE	201-220 (20)	2.000	
17	26.770	DAA_SLV_INFO_B6	0x0A	221-240 (20)	2.000	
18	28.770	DAA_SLV_INFO_B7	0xBE	241-260 (20)	2.000	
19	30.770	DAA_DADDR	0x10	261-278 (18)	2.000	

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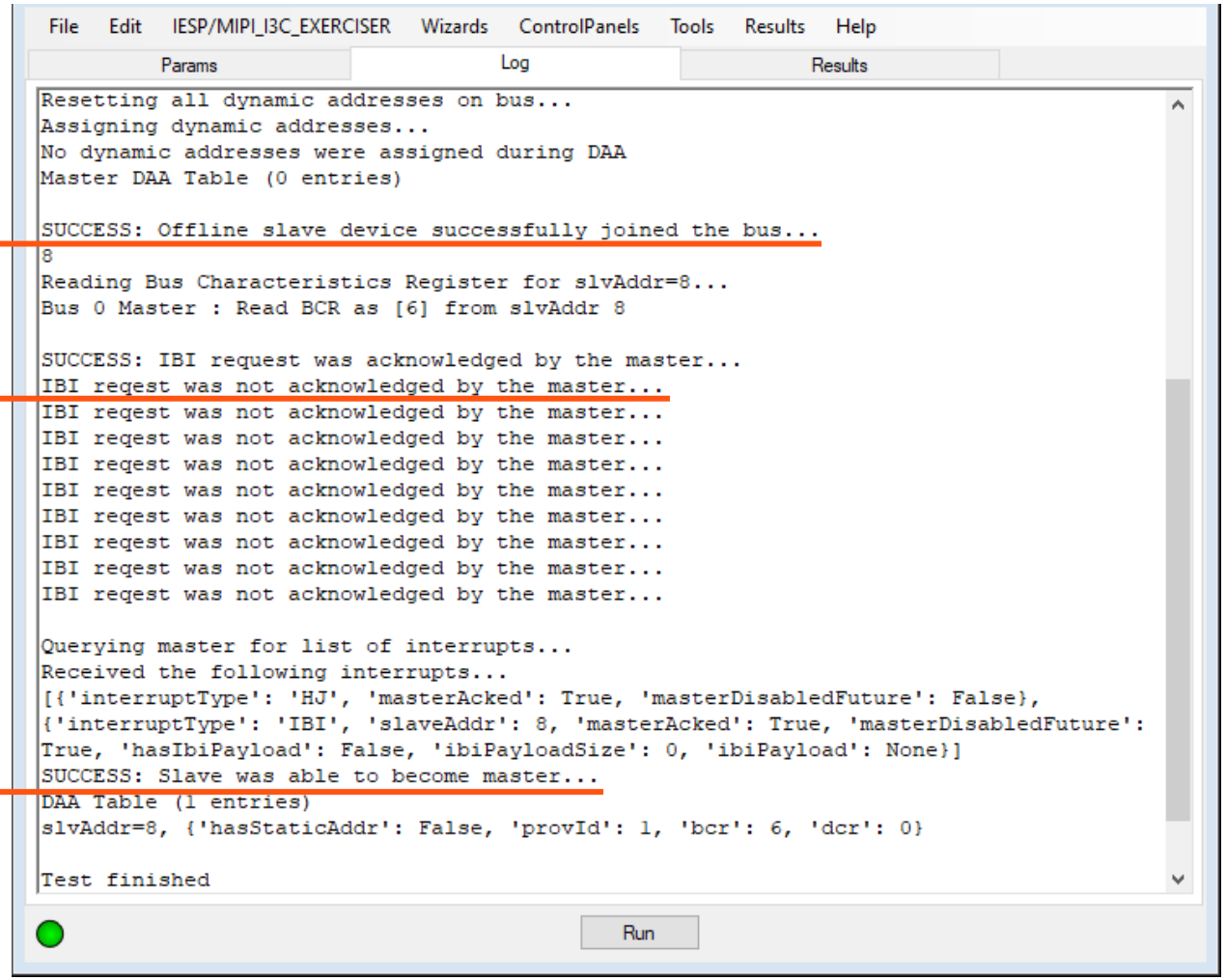
Powerful Scripting and Logging

Hot Join Example

Interrupt Example

Mastership Request Example



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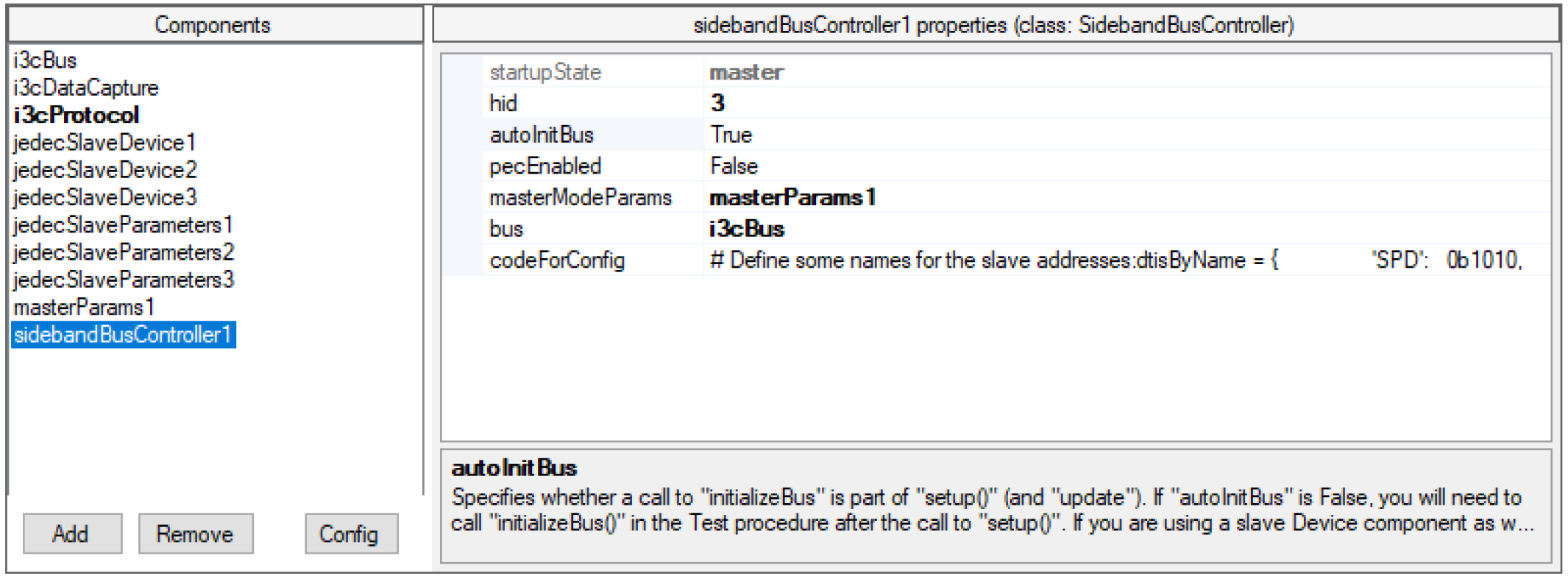
SidebandBus Controller Component



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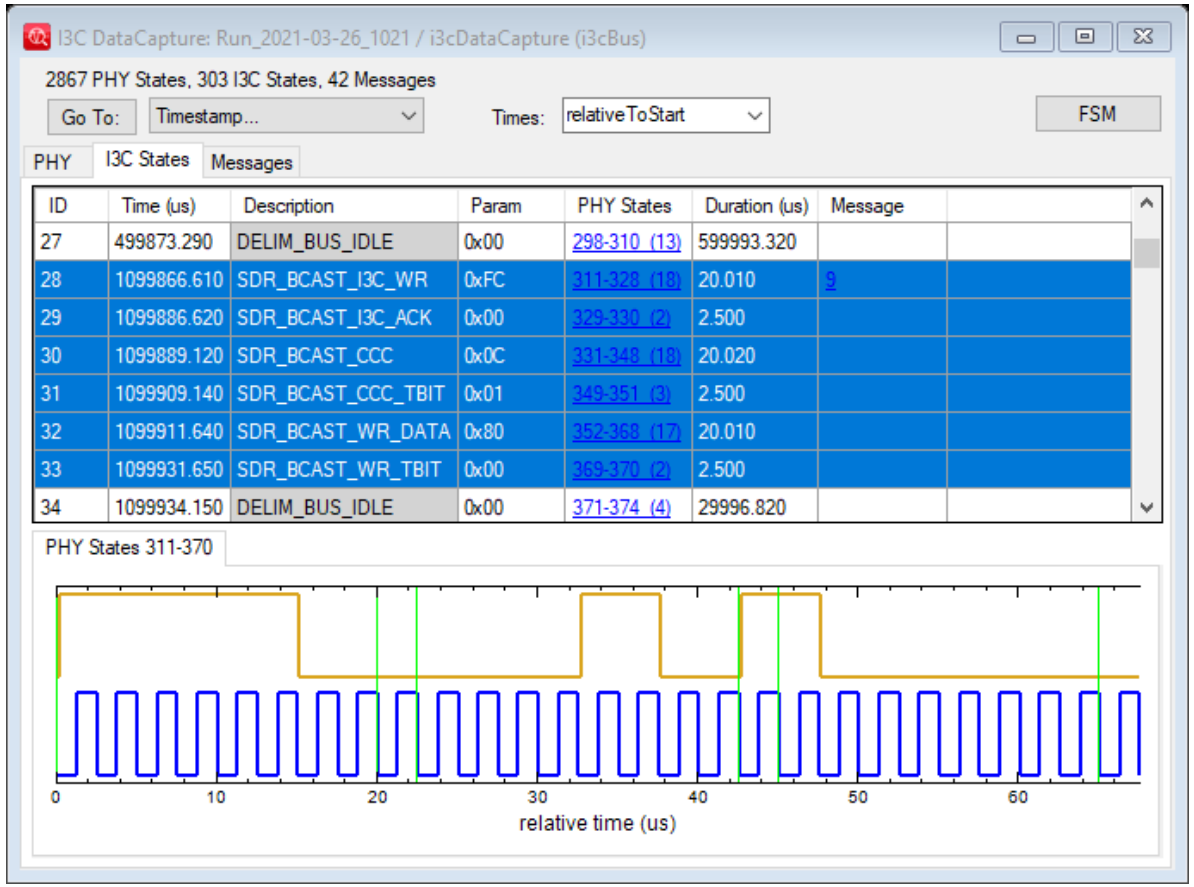
Example of Set Bus Config



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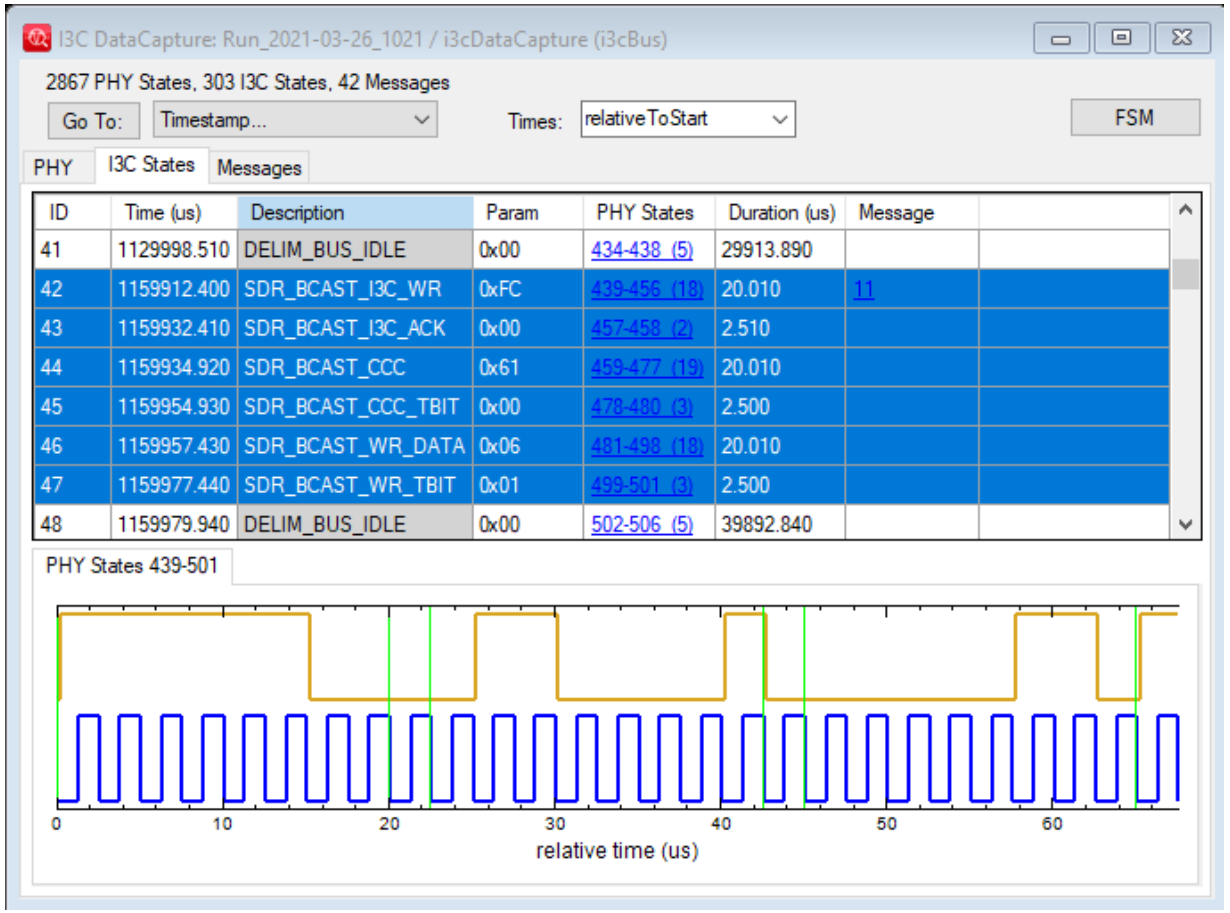
Example of SETHID



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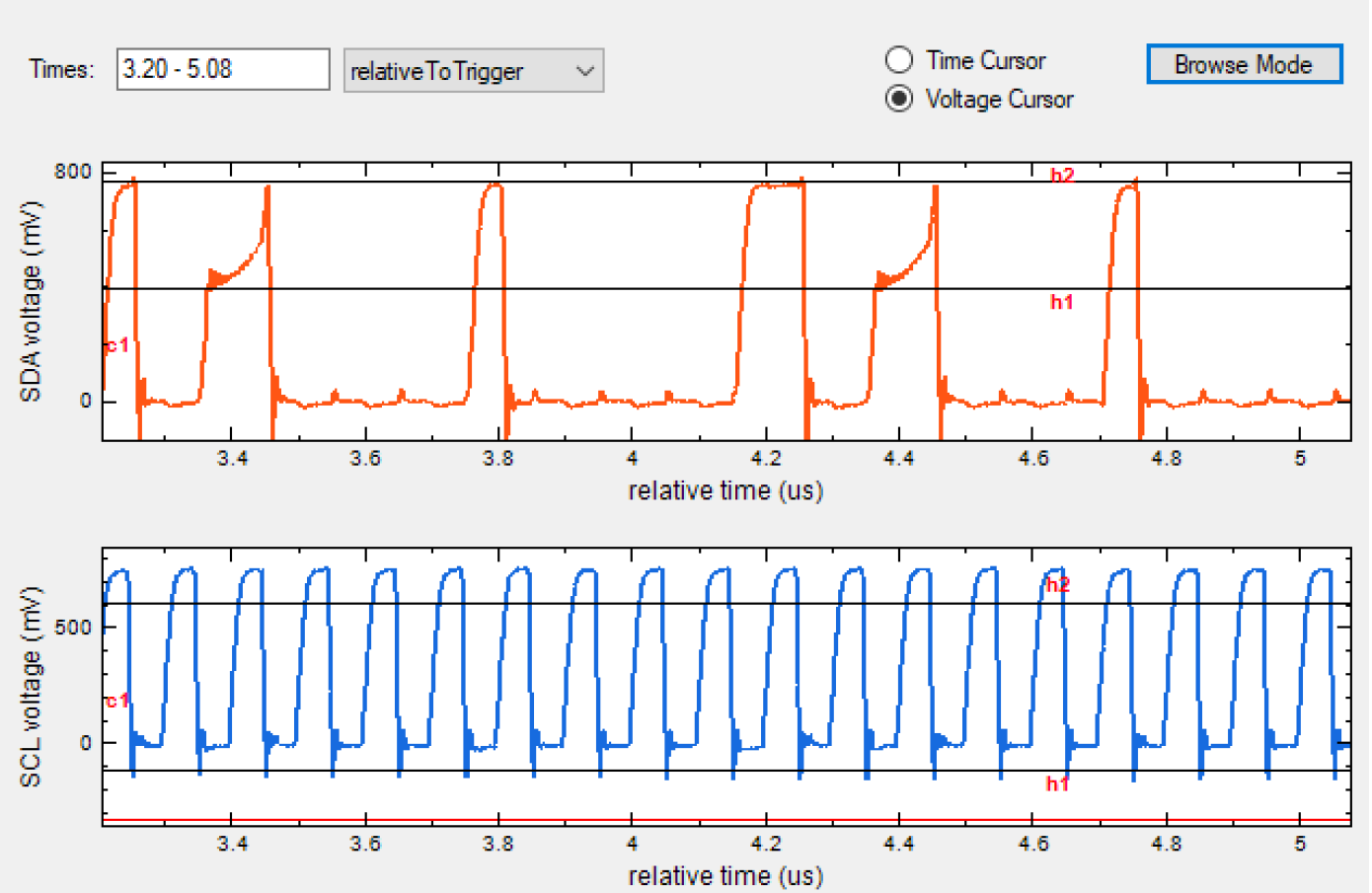
Real-Time, Single-Shot View of Signals

- I3C PurVue Analyzer™ embedded real-time oscilloscope license provides a real-time, single-shot view of all I3C signals
- It eliminates probing hassles with conventional scopes (attachment issues, cost issues, EMI issues) and completely eliminates the need for using a conventional scope



Pristine signal measurement is shown here where there are no artefacts due to the probes picking up noise from Wi-Fi or RF signals

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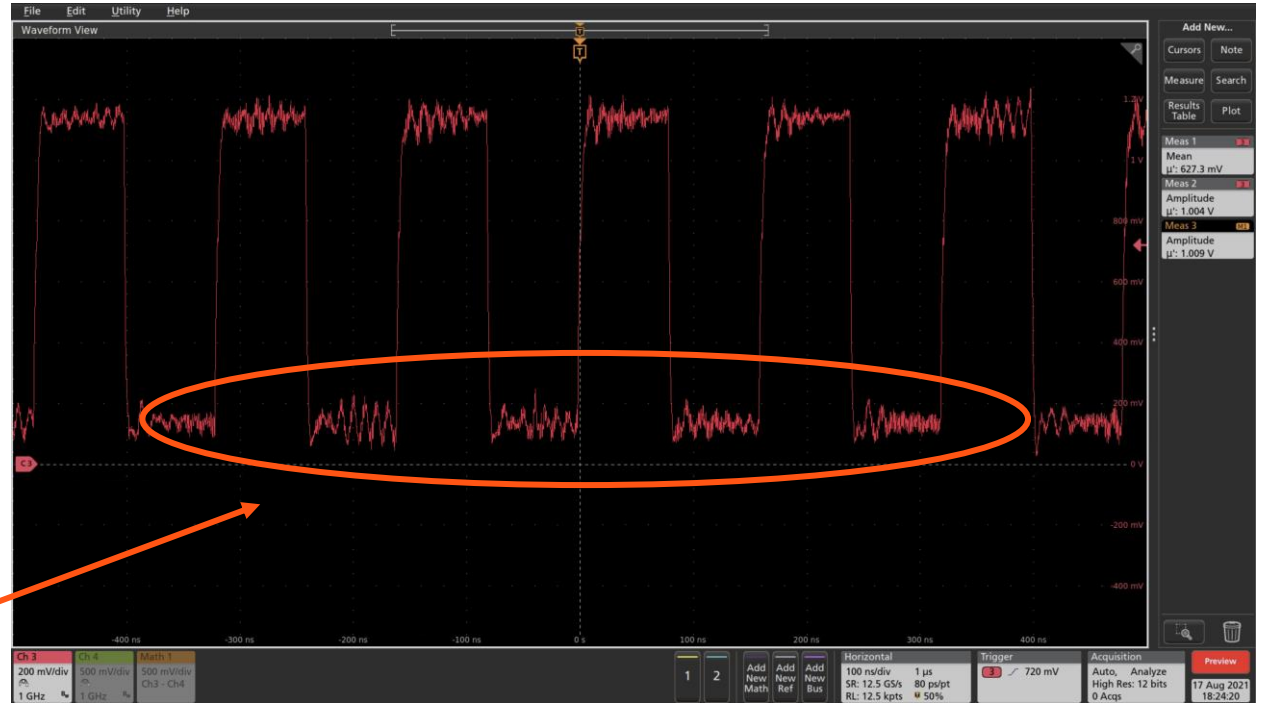
Why? Because Probes Are Antennas



Most oscilloscope probes result in too much noise pickup
The SV4E oscilloscope is embedded into the I3C signal plane, so it has far less noise

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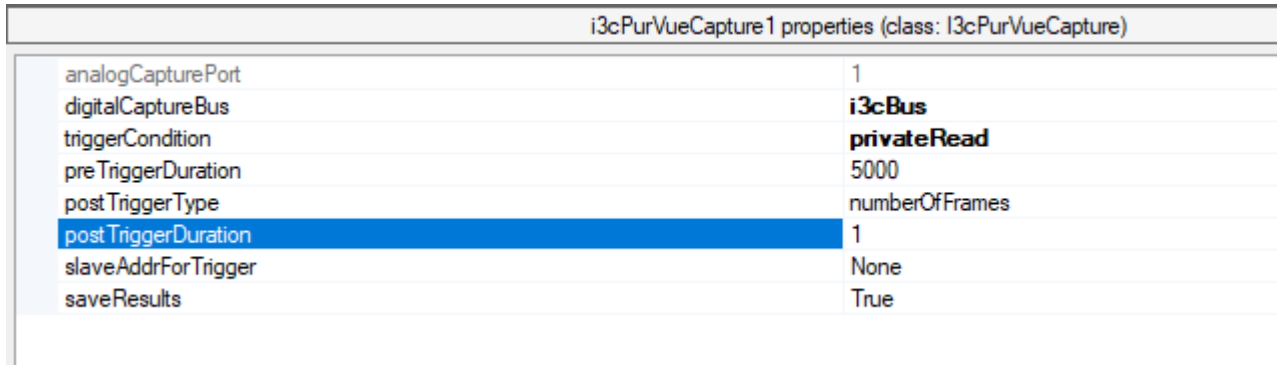
PurVue Analyzer™ Capture

- A single component for **simultaneous** protocol capture (digital capture) and oscilloscope capture (analog capture)
- Familiar user interface (the viewer is almost identical to the I3cDataCapture)
- With the PurVue viewer, users can quickly find interesting parts of the waveform since it is protocol-aware



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PurVue Analyzer™ Digital View

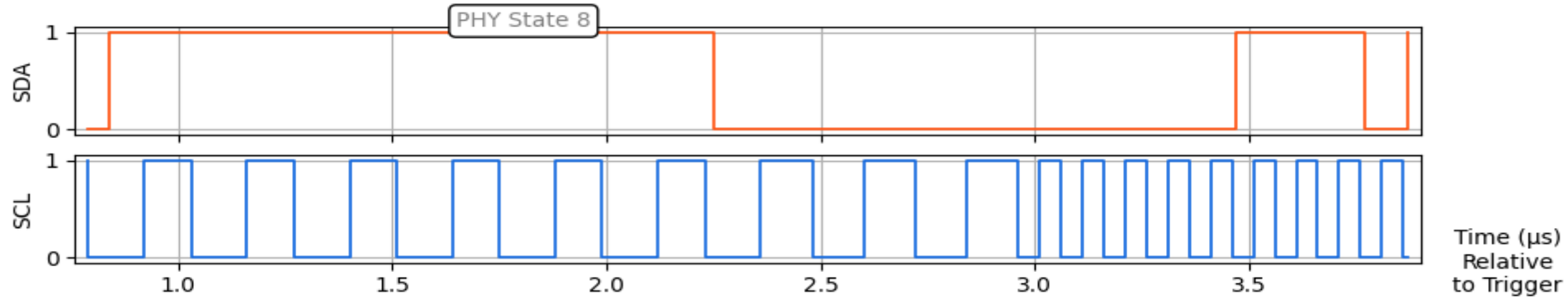
I3C PurVue Capture: Run_2022-08-08_1516 / i3cPurVueCapture1

274 PHY States, 21 I3C States, 1 Transactions Times: RelativeToTrigger

PHY | I3C States | Transactions

ID	Time (µs)	Description	Param	PHY States	Duration (µs)	Transaction	Info
0	0.000	DELIM_BUS_FREE	0x00	0-0 (1)	0.810		
1	0.810	SDR_BCAST_I3C_WR	0xFC	1-18 (18)	1.930	0	
2	2.740	SDR_BCAST_I3C_ACK	0x00	19-20 (2)	0.240		
3	2.980	SDR_CCC	0x07	21-38 (18)	0.800		CCC: ENTDAA
4	3.780	SDR_CCC_TBIT	0x00	39-41 (3)	0.100		
5	3.880	DAA_SR	0x00	42-45 (4)	1.650		
6	5.530	DAA_I3C_BCAST_RD	0xFD	46-64 (19)	0.800		
7	6.330	DAA_I3C_BCAST_ACK	0x00	65-66 (2)	0.240		
8	6.570	DAA_SLV_INFO_B0	0xCF	67-86 (20)	1.920		
9	8.490	DAA_SLV_INFO_B1	0x2A	87-108 (22)	1.920		

Digital Capture (PHY States 1-41) | Analog Capture



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PurVue Analyzer™ Analog View

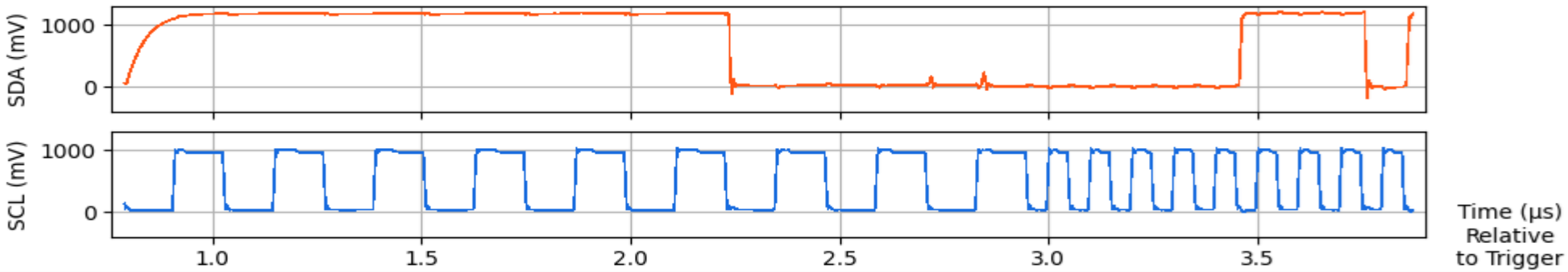
I3C PurVue Capture: Run_2022-08-08_1516 / i3cPurVueCapture1

274 PHY States, 21 I3C States, 1 Transactions Times: RelativeToTrigger

PHY | I3C States | Transactions

ID	Time (µs)	Description	Param	PHY States	Duration (µs)	Transaction	Info
0	0.000	DELIM_BUS_FREE	0x00	0-0 (1)	0.810		
1	0.810	SDR_BCAST_I3C_WR	0xFC	1-18 (18)	1.930	0	
2	2.740	SDR_BCAST_I3C_ACK	0x00	19-20 (2)	0.240		
3	2.980	SDR_CCC	0x07	21-38 (18)	0.800		CCC: ENTDAA
4	3.780	SDR_CCC_TBIT	0x00	39-41 (3)	0.100		
5	3.880	DAA_SR	0x00	42-45 (4)	1.650		
6	5.530	DAA_I3C_BCAST_RD	0xFD	46-64 (19)	0.800		
7	6.330	DAA_I3C_BCAST_ACK	0x00	65-66 (2)	0.240		
8	6.570	DAA_SLV_INFO_B0	0xCF	67-86 (20)	1.920		
9	8.490	DAA_SLV_INFO_B1	0x2A	87-108 (22)	1.920		

Digital Capture (PHY States 1-41) | Analog Capture



Notice how only the shape of the bottom waveform changes from last slide!

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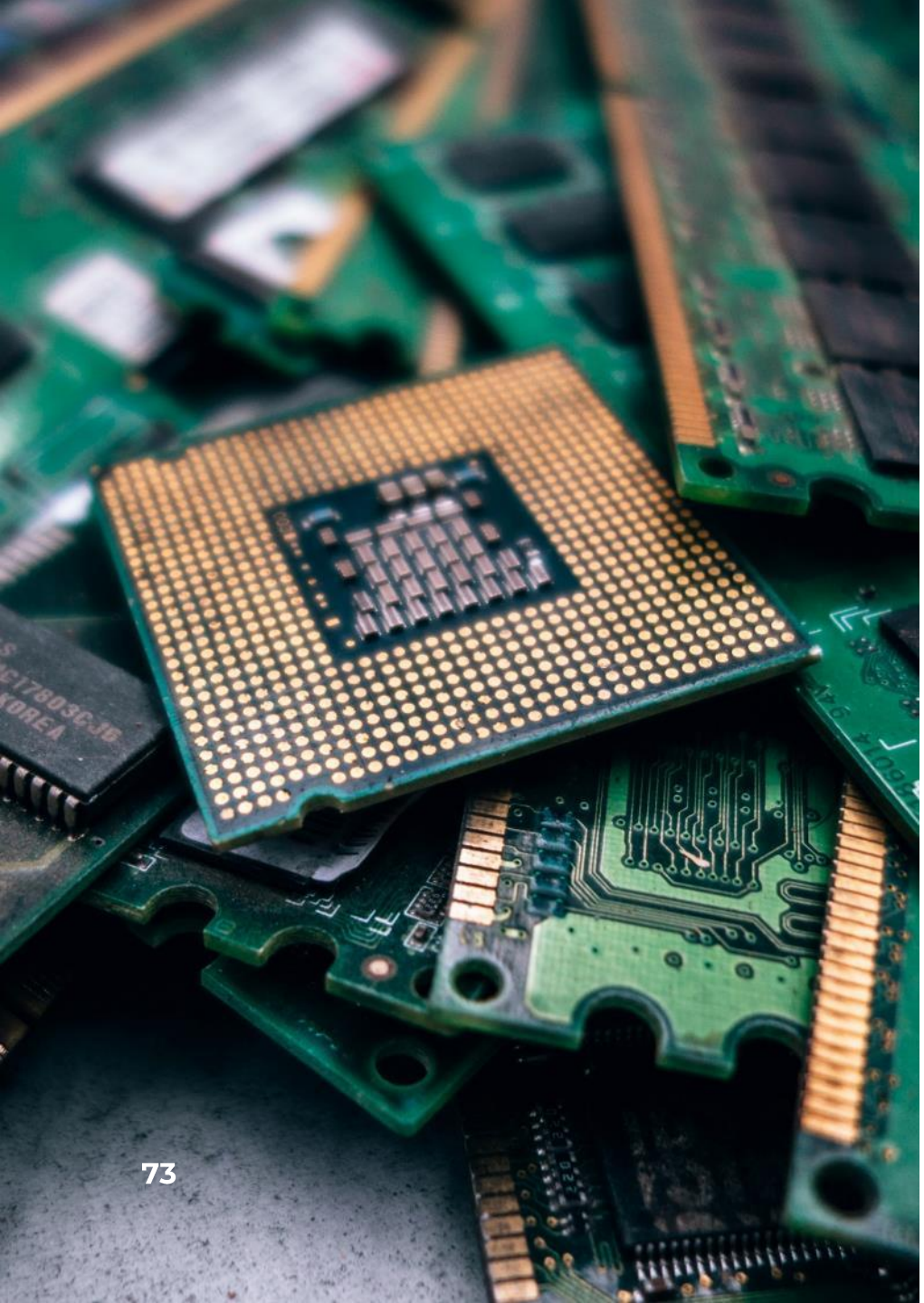

Summary

HIGHLY DIFFERENTIATED SOLUTIONS

- Introspect develops parallel test instruments for high-speed interfaces
- We have created a rich portfolio of solutions for source-synchronous and DDR interfaces
- Our solutions can be deployed at the component level and at the module level