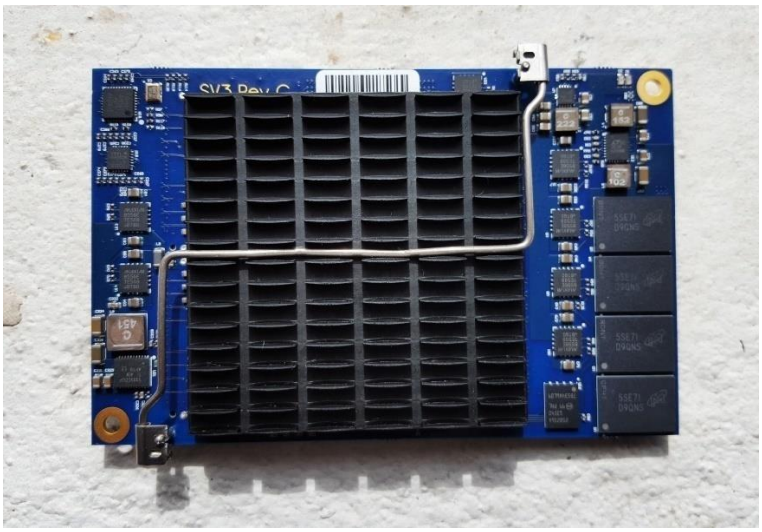
introspect technology

SV3D Support Logic Design Reference



Reference Design

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Introduction

Overview

The SV3DDirect-Attach SerDes Module is a versatile, high-performance instrument capable of receiver and transmitter validation at data rates up to 14Gbps, on up to 32 lanes simultaneously. It is designed to be readily integrated with test application or test boards providing test solutions to high speed SerDes interfaces, such as PCIe Gen3, MIPI M-PHY or USB3, with its state of the art digital data capture, bit error rate measurement, clock recovery, jitter decomposition and jitter generation functions. It also includes unique reconfiguration and protocol technologies that allow it to tackle multiple applications.

This document describes a proven reference carrier test board design and other peripheral circuits that can be served as a guide to building your test applications. The test board and support logic design described here are application-specific, and vary according to the specifications requirements and operation environment.

Content

- Ports and Connectors
- Connection Diagrams
- 12V Power Supply Generation
- Cooling Considerations
- I/O Connector Pin Out Information

Ports and Connectors

The SV3D is mounted on the load board using mezzanine connectors as described in a later section. In this section, we describe the various port types and how they map generally into the various connectors. For reference, a legend of available port types and corresponding connector locations is included in Figure 1.

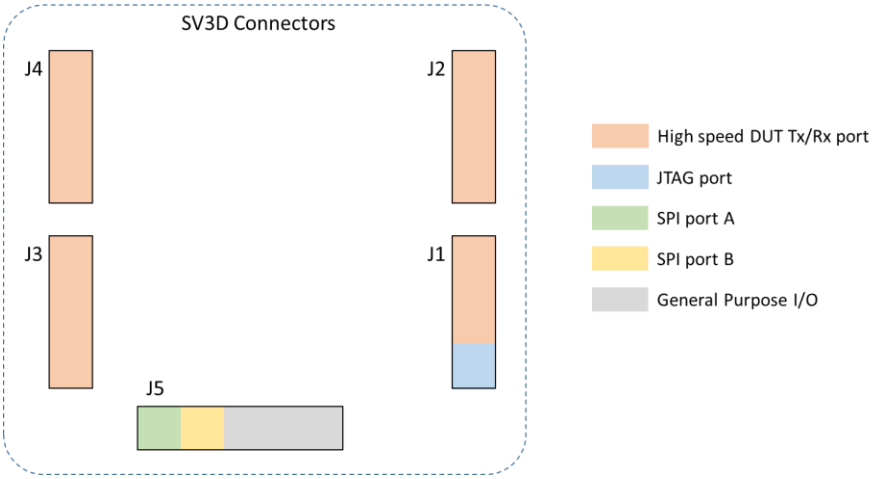

Figure 1 SV3D connector map and legend describing the different signal and control port types.

JTAG Port

The JTAG port is used for firmware update and debug. Its signals are routed on the J1 connector as per the following table:

Table 1 SV3D JTAG Connectors Pin-Out

Connector	Pin	Net
J1	16	JTAG Port: TMS
J1	30	JTAG Port: TCK
J1	31	JTAG Port: TDI
J1	45	JTAG Port: TDO

SPI Port A and Port B

The SV3D is controlled by two SPI ports facilitating commands to control the operation of the real time operating systems in the module. Table 2shows the pin assignment of the SPI port A and B on the J5 Samtec connector. Both SPI

ports act as slave. Port A controls the high-speed channel 1-16, and most of the global configuration, while port B controls the high-speed channel 17-32. Please refer to the *SV3 Command Interface Design Document* regarding the details of the SPI command interface.

Table 2 SV3D SPI Port A, B Connectors Pin-Out

Connector	Pin	Net	Connector	Pin	Net
J5	151	SPI Port A: SCLK	J5	166	SPI Port B: SCLK
J5	152	SPI Port A: MOSI	J5	161	SPI Port B: MOSI
J5	157	SPI Port A: MISO	J5	167	SPI Port B: MISO
J5	158	SPI Port A: SSN	J5	154	SPI Port B: SSN

High-Speed DUT Tx/Rx Port

This port consists of up to 32 differential transmitters and 32 differential receivers for connecting to devices under test. The pins on this port are distributed among 4 Molex connectors, J1 to J4, as described in detail later on in this document.

General Purpose I/O Port

Connector J5 contains a set of general purpose I/O signals that can be used for implementing custom vector programming or specialized functions, including two reconfigurable triggers and five flag capabilities for synchronizing with external tools or events. There is also a 12.5 MHz, 32 bit parallel interface available for transferring data to a DUT or external device. For further details and timing, please see the SV3D Direct-Attach SerDes Module datasheet.

The I/O level on this port is 2.5V LVCMOS, and the detailed pinout is described in Table 8 of this document

Connection Diagrams

JTAG Port Recommended Connections

The JTAG port is used for programming the firmware in the SV3D module. Thus, it is possible to leave all four pins of this port completely unconnected (N/C). However, the addition of a small header allows for updating firmware on the SV3D directly on the load board without having to remove it and place it on the SV3M carrier board. The recommended connection diagram for this header is shown in Figure 2. The connector shown is the LX60-12S connector from Hirose, and it is illustrated in Figure 3.

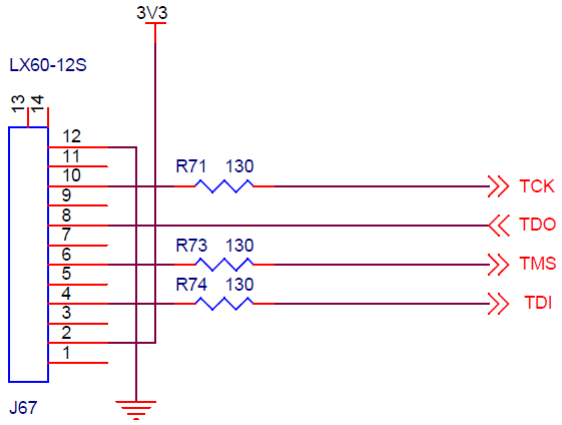

Figure 2 JTAG header connections.

Figure 3 Illustration of Hirose LX60-12S connector for attaching a JTAG firmware update cable.

SPI Port Recommended Connections

The simplest implementation of the SPI ports is to connect them directly to the ATE pin electronics as shown in Figure 4. There are important comments about this diagram:

- Each SPI port uses its own SSN line, so they are both connected in a point-to-point configuration with the ATE
- Related to the above comment, since each SPI slave of the SV3D is assumed to be connected directly to a corresponding SPI master on the ATE, each MISO line is not implemented as open-drain outputs but rather as a direct LVCMOS driver. This eliminates the need for implementing a pull-up resistor on this line

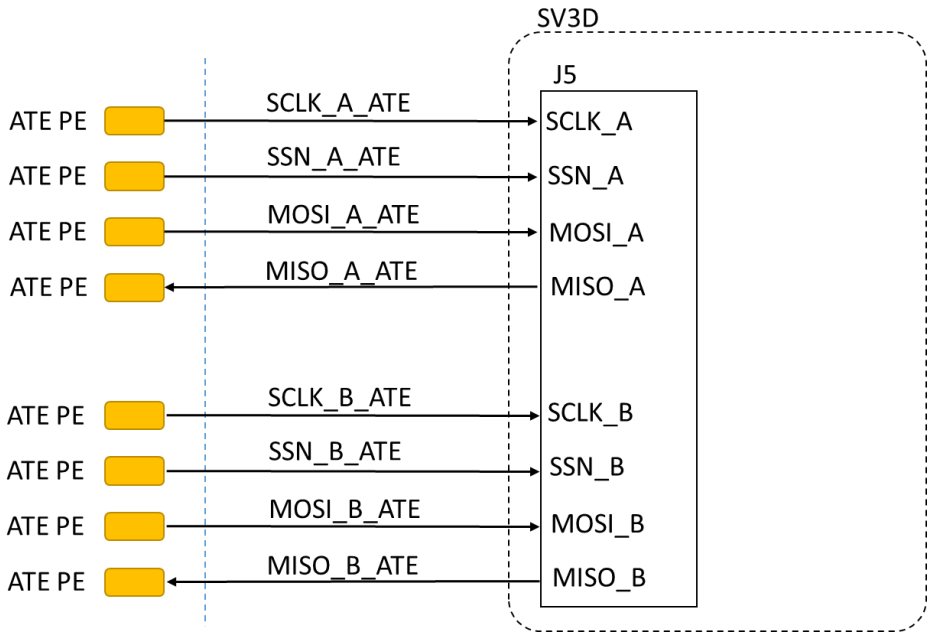

Figure 4 Simplest connection for the SPI A and SPI B ports.

Notwithstanding the simplest SPI connection described above, it is often required to perform debugging of the register programming steps in the production test program. Such debugging can be performed using the Introspect ESP Software, and it requires enabling a USB connection to the load board. Thus, it is highly desirable to implement the following USB-to-SPI converter solution on the load board. It consists of a commercial FTDI module that can be socketed into the load board as well as a simple switch for selecting between the ATE pin electronics of Figure 4 and the FTDI module. In the following discussion, please refer to Figure 5 to Figure 7 below.

In Figure 5, an illustration of the FTDI FT2232H module is shown. This is a commercial module that allows for transmitting SPI commands over a USB bus connected to a PC. The module can be socketed onto the load board, and it provides two independent SPI ports that are programmed using the Introspect ESP software. In terms of implementation on the load board, Figure 6 shows the electrical connections required by the FT2232H module. As can be seen, the module receives a 5V power supply from the load board. Of the various pins available on the module, 4 pins are used for SPI Port A and 4 are used for SPI Port B. Finally, there is a pin called SPI_ATE that controls a selection MUX described later. The SPI_ATE pin is programmed automatically in the Introspect ESP software. If the FT2232H module is not mounted on the load board, the SPI_ATE pin should be pulled up as shown in Figure 7. In this figure, a simple MUX solution is illustrated for selection between the ATE pin electronics and the FT2232H module. When the Introspect ESP software is attached, the FT2232H module is selected automatically through the SPI_ATE pin. Otherwise, the SPI_ATE pin is pulled up, which means that the ATE is used to drive the SPI ports on the SV3D module.

Figure 5 Illustration of the FT2232H USB-to-SPI converter module.

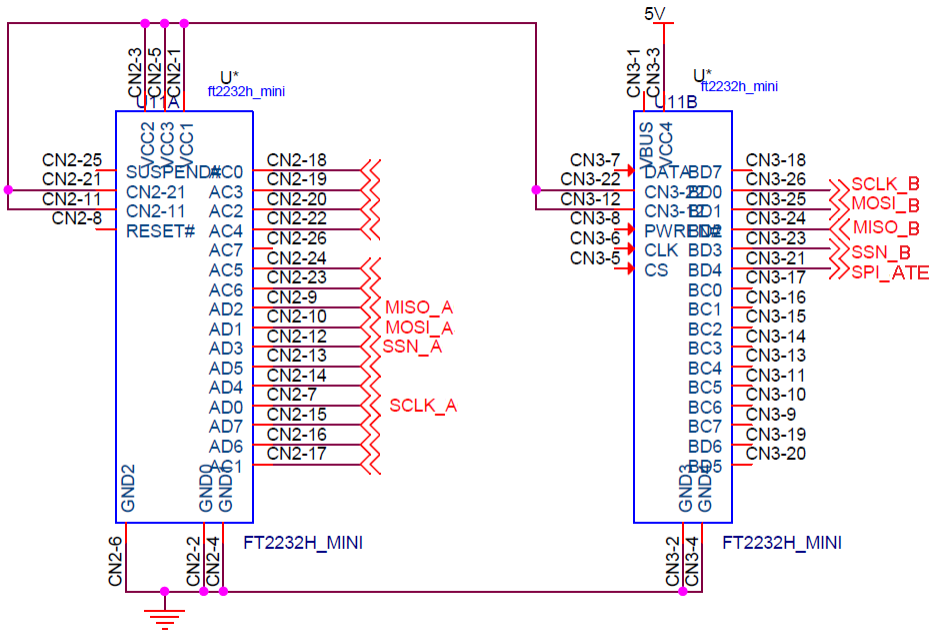

Figure 6 Schematic connections of the FT2232H module.

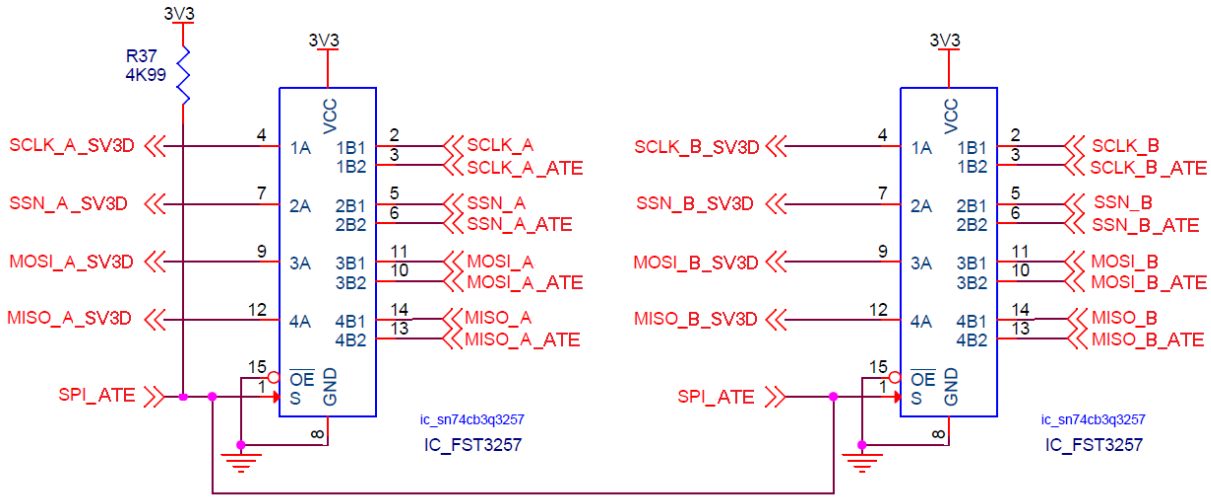

Figure 7 Schematic connections of the SPI selection switch.

Reference Clock Generation

Internal Clock Synthesis and External Clocks

The SV3D contains built-in clock synthesis (Figure 8) and does not require any external clock reference. For synchronization with ATE, an external reference clock input at frequency 25-250MHz is accepted (differential LVDS 3.3V). SPI commands program the multiplexer to select this reference source.

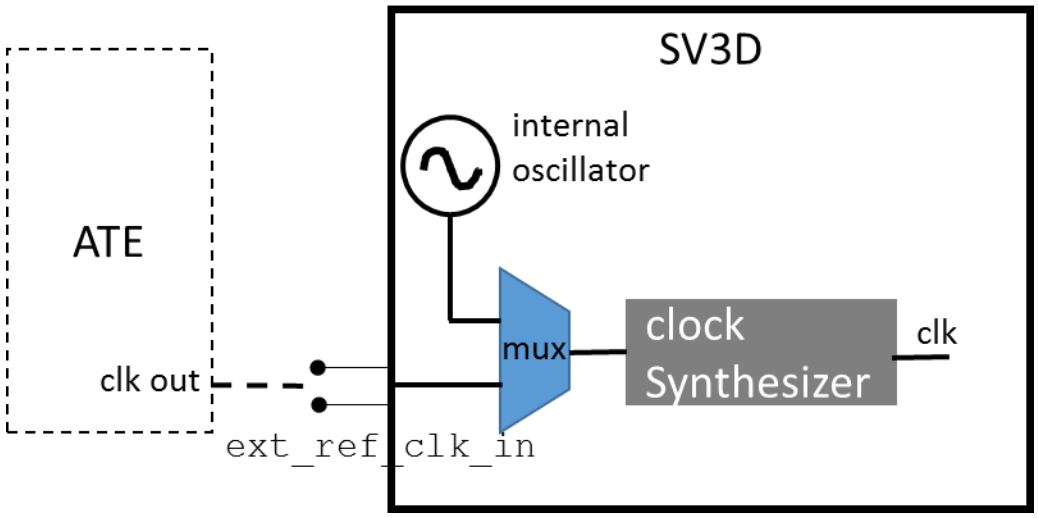

Figure 8 Reference clock circuit inside the SV3D.

12V Power Supply Generation

DC-DC Converter

The SV3D requires a single 12V supply.The supply voltage has to be between 9-13V. If a suitable supply is not available, a DC-DC converter can be used. For up conversion, an example design is illustrated in Figure 9. This circuit is based on the LTM8055 module.

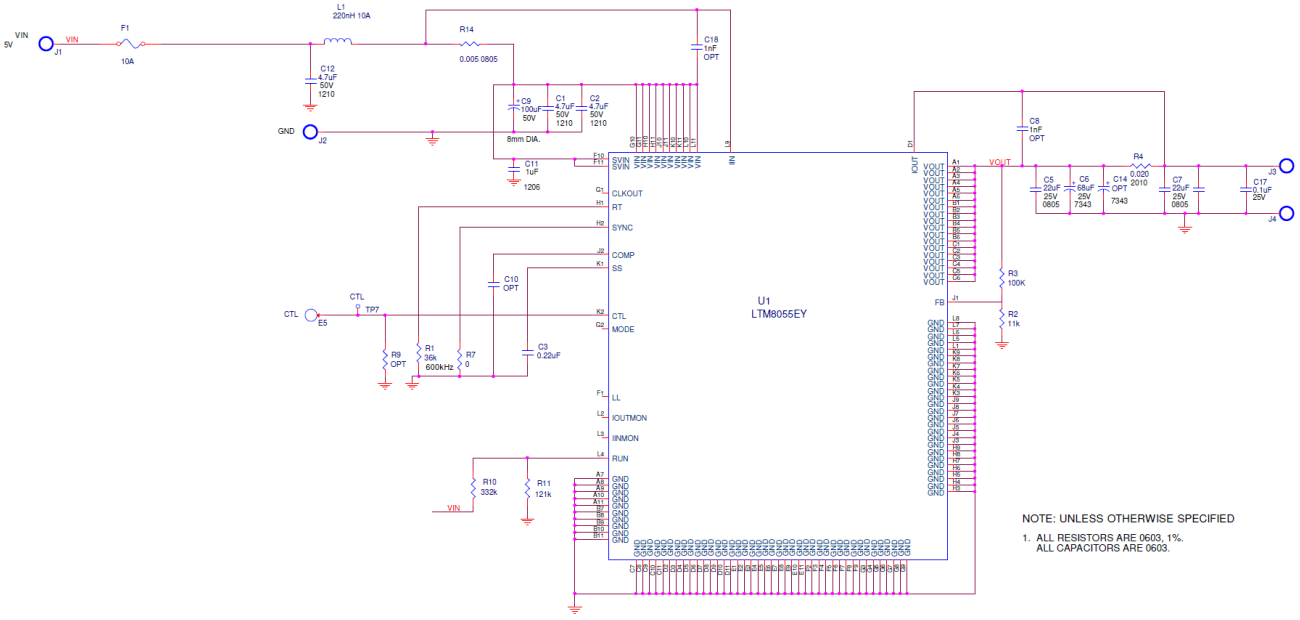

Figure 9 Example of deriving 12V from a 5V supply via aDC-DC converter.

An alternative design is based on the LTM4609 module shown in Figure 10. While this design is proven, it has certain deficiencies known to Linear Technology. Namely, the internal converter skips one cycle out of ten. So, if there is not enough filtering on the input line, some noise might inject back into the input power supply. It is important that the highlighted filter values are applied.

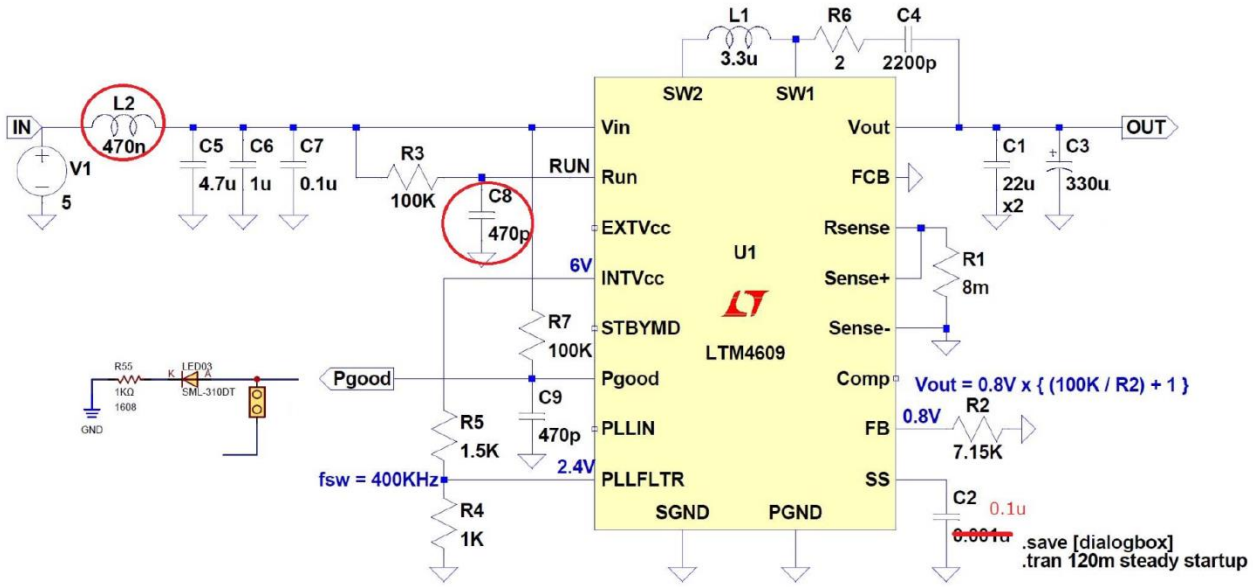

Figure 10 Alternative power module design.

Cooling Considerations

Fans

Typically, mechanical constraints dictate the selection and placement of the cooling fans. A 12V fan with at least 4.0 CFM is required for cooling purposes. Introspect uses the *Delta Electronics BFB03512HHA-AF00* mounted on 0.500" standoffs to push air through the SV3D heat sink. A fan or set of fans, can be placed at either end of the SV3D heat sink forcing air in **one direction** over the cooling fins as shown in Figure 11 and Figure 12.

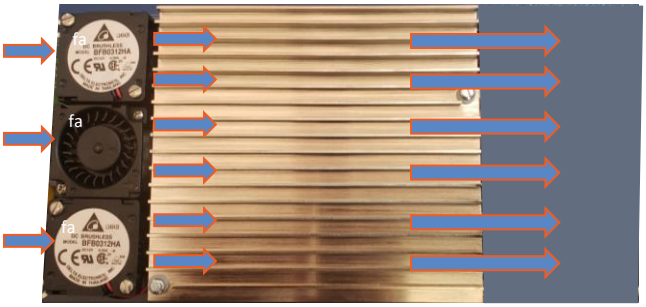

*Figure 11 Fans mounted on one side of SV3D module for horizontal airflow in **one direction***

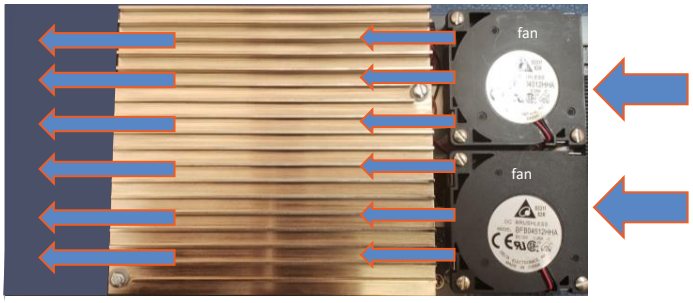

*Figure 12 Fans mounted on other side of SV3D module for horizontal airflow in **one direction***

Physical and Electrical Interface

Physical Appearance

Figure 13 and Figure 14 depict the top and bottom views of the SV3D module.

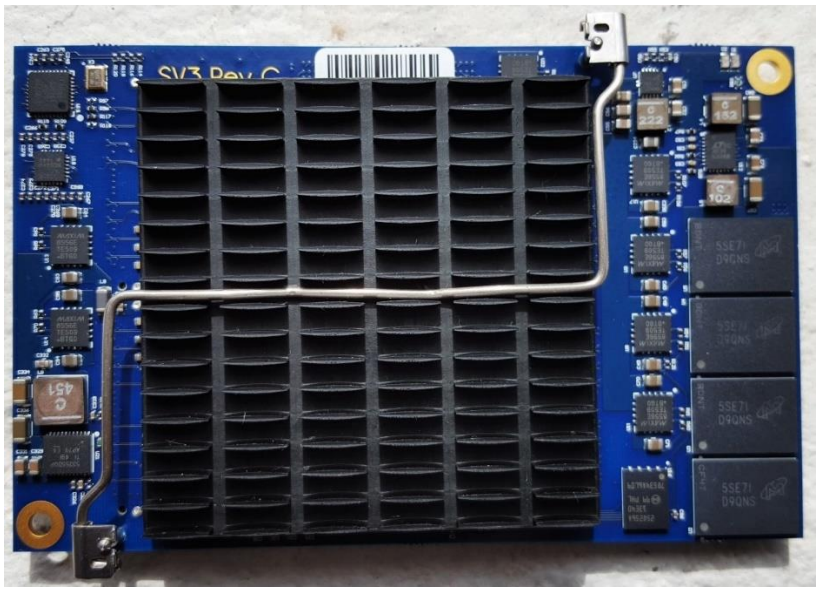

Figure 13 Top view of SV3D module

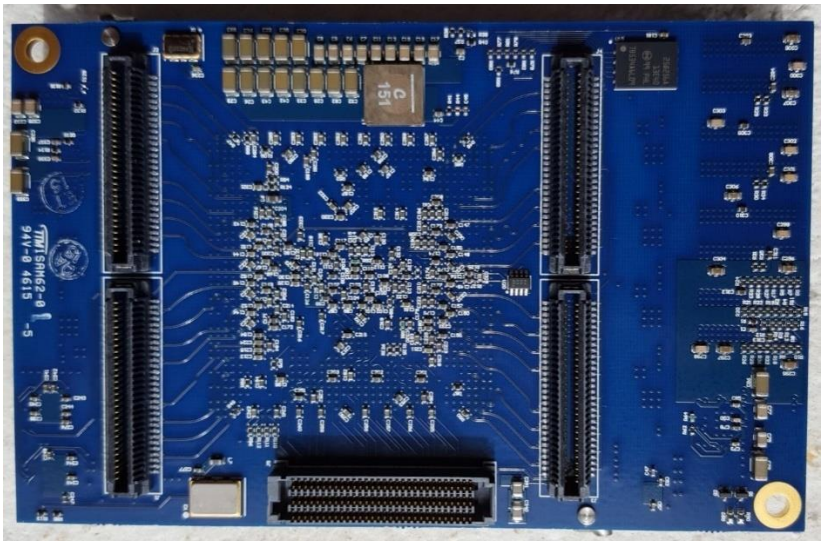

Figure 14 Bottom view of SV3D module

Load board Connectors Footprint and Dimensions

Figure 15 depicts the connectors footprint required to mate with the SV3D module. The rectangle outline is occupied by the SV3D module, to be mounted on the load board by 2 diagonal mounting holes and 5 connectors J1, J2, J3, J4 and J5.

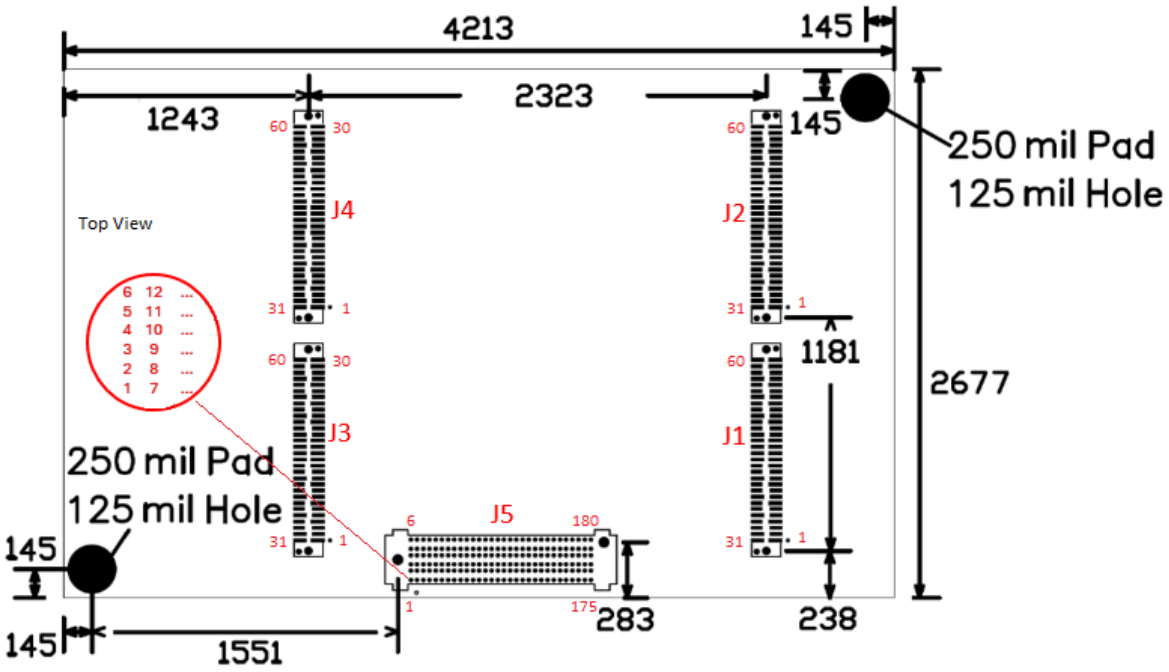

Figure 15 SV3D load board footprint placement. Measurements are in mil.

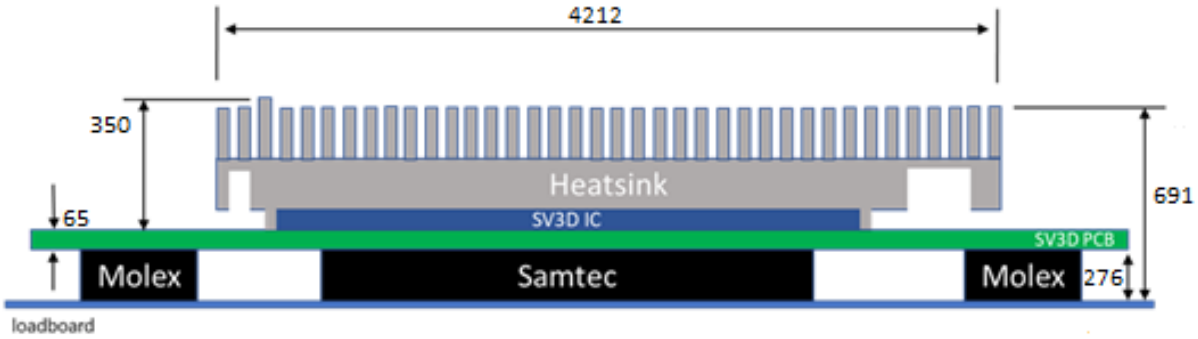

Figure 16 SV3D side profile on load board. Measurements are in mil.

The connectors part number information is shown in Table 3.

Table 3 Load board Connectors Descriptions

Connector	Manufacturer	Part Number	Descriptions	Pin Count
J1, J2, J3, J4	Molex	171446 -1115 (or -0115)	SPEEDSTACK PLUG ASSY,30CKT,3MM	60
J5	Samtec	SEAM8-30-S02.0-S-06-3	CONN SEARAY 30x6, 0.8mm pitch	180

Connectors Pin Out

The following tables describe the pin out information of the 5 connectors on the SV3D depicted in Figure 15. When designing the interface logic, please ensure not to drive any I/O pins on the SV3D until the power rails have been completely powered on.

Table 4 Load board J1 Connector Pin-Out (connects to ref. design schematic J58)

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	RX17_P	GXB Receive Link	1.5V PCML
3	RX17_N	GXB Receive Link	1.5V PCML
5	RX21_P	GXB Receive Link	1.5V PCML
6	RX21_N	GXB Receive Link	1.5V PCML
8	RX18_P	GXB Receive Link	1.5V PCML
9	RX18_N	GXB Receive Link	1.5V PCML
11	RX19_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
12	RX19_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
14	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	JTAG-TMS	Built-in Pull-up Resistor10kOhm	2.5V
18	RX20_P	GXB Receive Link	1.5V PCML
19	RX20_N	GXB Receive Link	1.5V PCML
21	RX24_N	GXB Receive Link	1.5V PCML
22	RX24_P	GXB Receive Link	1.5V PCML
24	RX23_N	GXB Receive Link	1.5V PCML
25	RX23_P	GXB Receive Link	1.5V PCML
27	RX22_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
28	RX22_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
30	JTAG-TCK	Built-in Pull-up Resistor 1kOhm	2.5V
31	JTAG-TDI	Built-in Pull-up Resistor 10kOhm	2.5V
33	TX17_P	GXB Transmit Link	1.5V PCML
34	TX17_N	GXB Transmit Link	1.5V PCML
36	TX21_P	GXB Transmit Link	1.5V PCML
37	TX21_N	GXB Transmit Link	1.5V PCML
39	TX18_N	GXB Transmit Link	1.5V PCML
40	TX18_P	GXB Transmit Link	1.5V PCML
42	TX19_P	GXB Transmit Link	1.5V PCML
43	TX19_N	GXB Transmit Link	1.5V PCML
45	JTAG-TDO	Built-in Pull-up Resistor 21.5kOhm	2.5V
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	TX20_N	GXB Transmit Link	1.5V PCML
50	TX20_P	GXB Transmit Link	1.5V PCML
52	TX24_P	GXB Transmit Link	1.5V PCML
53	TX24_N	GXB Transmit Link	1.5V PCML
55	TX23_N	GXB Transmit Link	1.5V PCML
56	TX23_P	GXB Transmit Link	1.5V PCML
58	TX22_P	GXB Transmit Link	1.5V PCML
59	TX22_N	GXB Transmit Link	1.5V PCML

Table 5 Load board J2 Connector Pin-Out (connects to ref. design schematic J57)

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	RX25_P	GXB Receive Link	1.5V PCML
3	RX25_N	GXB Receive Link	1.5V PCML

5	RX29_P	GXB Receive Link	1.5V PCML
6	RX29_N	GXB Receive Link	1.5V PCML
8	RX26_P	GXB Receive Link	1.5V PCML
9	RX26_N	GXB Receive Link	1.5V PCML
11	RX30_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
12	RX30_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
14	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	EXTRA_IO_1	GPIO pin	2.5V LVCMOS
18	RX27_P	GXB Receive Link	1.5V PCML
19	RX27_N	GXB Receive Link	1.5V PCML
21	RX31_P	GXB Receive Link	1.5V PCML
22	RX31_N	GXB Receive Link	1.5V PCML
24	RX28_P	GXB Receive Link	1.5V PCML
25	RX28_N	GXB Receive Link	1.5V PCML
27	RX32_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
28	RX32_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
30	EXTRA_IO_3	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_0	GPIO pin	2.5V LVCMOS
33	TX25_N	GXB Transmit Link	1.5V PCML
34	TX25_P	GXB Transmit Link	1.5V PCML
36	TX29_P	GXB Transmit Link	1.5V PCML
37	TX29_N	GXB Transmit Link	1.5V PCML
39	TX26_N	GXB Transmit Link	1.5V PCML
40	TX26_P	GXB Transmit Link	1.5V PCML
42	TX30_P	GXB Transmit Link	1.5V PCML
43	TX30_N	GXB Transmit Link	1.5V PCML
45	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	EXTRA_IO_2	GPIO pin	2.5V LVCMOS
49	TX27_N	GXB Transmit Link	1.5V PCML
50	TX27_P	GXB Transmit Link	1.5V PCML
52	TX31_P	GXB Transmit Link	1.5V PCML
53	TX31_N	GXB Transmit Link	1.5V PCML
55	TX28_N	GXB Transmit Link	1.5V PCML
56	TX28_P	GXB Transmit Link	1.5V PCML
58	TX32_P	GXB Transmit Link	1.5V PCML
59	TX32_N	GXB Transmit Link	1.5V PCML

Table 6 Load board J3 Connector Pin-Out (connects to ref. design schematic J55)

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	TX1_P	GXB Transmit Link	1.5V PCML
3	TX1_N	GXB Transmit Link	1.5V PCML
5	TX2_P	GXB Transmit Link	1.5V PCML
6	TX2_N	GXB Transmit Link	1.5V PCML
8	TX3_N	GXB Transmit Link	1.5V PCML
9	TX3_P	GXB Transmit Link	1.5V PCML
11	TX4_P	GXB Transmit Link	1.5V PCML
12	TX4_N	GXB Transmit Link	1.5V PCML
14	EXTRA_IO_5	Master and Slave Cores Locked. Active Low	2.5V LVCMOS
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
18	TX8_N	GXB Transmit Link	1.5V PCML
19	TX8_P	GXB Transmit Link	1.5V PCML
21	TX7_N	GXB Transmit Link	1.5V PCML
22	TX7_P	GXB Transmit Link	1.5V PCML
24	TX6_N	GXB Transmit Link	1.5V PCML
25	TX6_P	GXB Transmit Link	1.5V PCML
27	TX5_N	GXB Transmit Link	1.5V PCML
28	TX5_P	GXB Transmit Link	1.5V PCML
30	EXTRA_IO_7	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_4	User LED and Tx Buffer Underflow. Active Low	2.5V LVCMOS

33	RX1_P	GXB Receive Link	1.5V PCML
34	RX1_N	GXB Receive Link	1.5V PCML
36	RX2_N	GXB Receive Link	1.5V PCML
37	RX2_P	GXB Receive Link	1.5V PCML
39	RX3_P	GXB Receive Link	1.5V PCML
40	RX3_N	GXB Receive Link	1.5V PCML
42	RX4_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
43	RX4_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
45	EXTRA_IO_6	Master and Slave Cores Ready. Active Low	2.5V LVCMOS
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	RX8_P	GXB Receive Link	1.5V PCML
50	RX8_N	GXB Receive Link	1.5V PCML
52	RX7_N	GXB Receive Link	1.5V PCML
53	RX7_P	GXB Receive Link	1.5V PCML
55	RX6_P	GXB Receive Link	1.5V PCML
56	RX6_N	GXB Receive Link	1.5V PCML
58	RX5_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
59	RX5_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML

Table 7 Load board J4 Connector Pin-Out (connects to ref. design schematic J56)

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	TX9_P	GXB Transmit Link	1.5V PCML
3	TX9_N	GXB Transmit Link	1.5V PCML
5	TX10_P	GXB Transmit Link	1.5V PCML
6	TX10_N	GXB Transmit Link	1.5V PCML
8	TX14_N	GXB Transmit Link	1.5V PCML
9	TX14_P	GXB Transmit Link	1.5V PCML
11	TX13_N	GXB Transmit Link	1.5V PCML
12	TX13_P	GXB Transmit Link	1.5V PCML
14	REFIN_CLK_P	Ref Clock Input	3.3V LVDS*
15	REFIN_CLK_N	Ref Clock Input	3.3V LVDS*
16	EXTRA_IO_9	GPIO pin	2.5V LVCMOS
18	TX11_P	GXB Transmit Link	1.5V PCML
19	TX11_N	GXB Transmit Link	1.5V PCML
21	TX15_P	GXB Transmit Link	1.5V PCML
22	TX15_N	GXB Transmit Link	1.5V PCML
24	TX12_P	GXB Transmit Link	1.5V PCML
25	TX12_N	GXB Transmit Link	1.5V PCML
27	TX16_N	GXB Transmit Link	1.5V PCML
28	TX16_P	GXB Transmit Link	1.5V PCML
30	EXTRA_IO_11	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_8	GPIO pin	2.5V LVCMOS
33	RX9_P	GXB Receive Link	1.5V PCML
34	RX9_N	GXB Receive Link	1.5V PCML
36	RX10_N	GXB Receive Link	1.5V PCML
37	RX10_P	GXB Receive Link	1.5V PCML
39	RX14_P	GXB Receive Link	1.5V PCML
40	RX14_N	GXB Receive Link	1.5V PCML
42	RX13_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
43	RX13_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
45	EXTRA_IO_10	GPIO pin	2.5V LVCMOS
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	RX11_N	GXB Receive Link	1.5V PCML
50	RX11_P	GXB Receive Link	1.5V PCML
52	RX15_P	GXB Receive Link	1.5V PCML
53	RX15_N	GXB Receive Link	1.5V PCML
55	RX12_N	GXB Receive Link	1.5V PCML
56	RX12_P	GXB Receive Link	1.5V PCML
58	RX16_P	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML
59	RX16_N	GXB Receive Link, not present in SV3D09 firmware	1.5V PCML

** REFIN_CLK_P and REFIN_CLK_N have internal AC coupling.*

Table 8 Load board J5 Connector Pin-Out (connects to ref. design schematic J59)*

Pin	Net	Pin	Net	Pin	Net
1	12V0	61	PTI_RESET_N	121	GPIO_1_0 / FLAG[3]
2	12V0	62	GPIO_4_4 / Reserved	122	GPIO_1_7
3	12V0	63	GPIO_4_11 / Reserved	123	GND
4	12V0	64	GPIO_4_12 / Reserved	124	GPIO_2_12
5	12V0	65	GPIO_4_19 / Reserved	125	GPIO_2_19
6	12V0	66	GND	126	GPIO_2_20
7	GND	67	GPIO_3_0 / Reserved	127	GPIO_1_1
8	GND	68	GPIO_3_7 / Reserved	128	GND
9	GND	69	GPIO_3_8 / Reserved	129	GPIO_DQS_1_8
10	GND	70	GPIO_3_15 / Reserved	130	GPIO_1_15
11	GND	71	GND	131	GPIO_1_16
12	GND	72	GPIO_4_20 / Reserved	132	GPIO_1_23
13	PTI_DATA_0	73	GPIO_3_1	133	GND
14	PTI_DATA_1	74	GPIO_3_6	134	GPIO_1_6
15	PTI_DATA_2	75	GPIO_3_9	135	GPIO_1_9
16	PTI_DATA_3	76	GND	136	GPIO_1_14
17	PTI_DATA_4	77	GPIO_3_16	137	GPIO_1_17
18	PTI_DATA_5	78	GPIO_3_23	138	GPIO_1_22
19	PTI_DATA_6	79	GPIO_3_2	139	GPIO_1_2 / EXT_TRIG[1]
20	PTI_DATA_7	80	GPIO_DQS_3_5	140	GPIO_1_5 / FLAG[2]
21	PTI_DATA_8	81	GND	141	GPIO_1_10
22	GPIO_5_14	82	GPIO_3_14	142	GPIO_DQS_1_13
23	GPIO_5_17	83	GPIO_DQS_3_17	143	GPIO_1_18
24	GND	84	GPIO_3_22	144	GPIO_1_21
25	PTI_DATA_9	85	GPIO_3_3	145	GPIO_1_3 / FLAG[1]
26	PTI_DATA_10	86	GND	146	GPIO_1_4 / FLAG[0]
27	PTI_DATA_11	87	GPIO_3_10	147	GPIO_1_11
28	PTI_DATA_12	88	GPIO_3_13	148	GPIO_1_12
29	GND	89	GPIO_3_18	149	GPIO_1_19
30	PTI_DATA_13	90	GPIO_3_21	150	GND
31	PTI_DATA_14	91	GND	151	GPIO_0_0 / SPI PortA SCLK
32	PTI_DATA_15	92	GPIO_3_4	152	GPIO_0_7 / SPI PortA MOSI
33	PTI_DATA_16	93	GPIO_3_11	153	GPIO_0_8
34	GND	94	GPIO_3_12	154	GPIO_0_15 / SPI PortB SSN
35	PTI_DATA_17	95	GPIO_3_19	155	GND
36	PTI_DATA_18	96	GPIO_3_20	156	GPIO_1_20
37	PTI_DATA_19	97	GPIO_2_0	157	GPIO_0_1 / SPI PortA MISO
38	PTI_DATA_20	98	GPIO_DQS_2_7	158	GPIO_0_6 / SPI PortA SSN
39	GND	99	GPIO_2_8	159	GPIO_DQS_0_9
40	PTI_DATA_21	100	GPIO_2_15	160	GND
41	PTI_DATA_22	101	GPIO_2_16	161	GPIO_0_16 / SPI PortB MOSI
42	PTI_DATA_23	102	GPIO_2_23	162	GPIO_0_23
43	PTI_DATA_24	103	GPIO_2_1	163	GPIO_0_2
44	GND	104	GPIO_2_6	164	GPIO_0_5
45	PTI_DATA_25	105	GPIO_2_9	165	GND
46	PTI_DATA_26	106	GPIO_DQS_2_14	166	GPIO_0_14 / SPI PortB SCLK
47	PTI_DATA_27	107	GPIO_2_17	167	GPIO_0_17 / SPI PortB MISO
48	PTI_DATA_28	108	GND	168	GPIO_0_22
49	GND	109	GPIO_2_2	169	GPIO_0_3
50	PTI_DATA_29	110	GPIO_2_5	170	GND
51	PTI_DATA_30	111	GPIO_2_10	171	GPIO_0_10
52	PTI_DATA_31	112	GPIO_2_13	172	GPIO_0_13
53	PTI_CLK	113	GND	173	GPIO_0_18
54	PTI_WRREQ_N	114	GPIO_2_22	174	GPIO_0_21
55	PTI_RDREQ_N	115	GPIO_2_3 / EXT_TRIG[0]	175	GND
56	PTI_WR_N	116	GPIO_2_4 / FLAG[4]	176	GPIO_0_4
57	PTI_RD_N	117	GPIO_2_11	177	GPIO_0_11
58	CMD_PROC_READY_A	118	GND	178	GPIO_0_12
59	CMD_PROC_READY_B	119	GPIO_2_18	179	SV3_RST_N
60	PTI_OE_N	120	GPIO_2_21	180	GPIO_DQS_0_20

Revision Number	History	Date
1.0	Revised document release	Jul 27, 2016
1.1	Added ports and connectors section; added recommended connection diagrams; updated pinout table; corrected J1-J4 locations	Aug 2, 2016
1.2	Update fan specs, connector part numbers, table 4-7	Nov 11, 2016
1.3	Updates to pinout (flags, triggers, and PTI interface).	Feb 14, 2017
1.4	Clarification to figures and pinouts	Mar 10, 2017
1.5	Removed figure for vertical cooling; changed figures for horizontal cooling; updated figure 16 dimensions	Jun 19, 2018
1.6	Updated J5 Pinout Table	Nov 14, 2023
1.7	Updated Figure 15 with additional pin numbering information. Updated J5 connector part number.	April 4, 2024

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