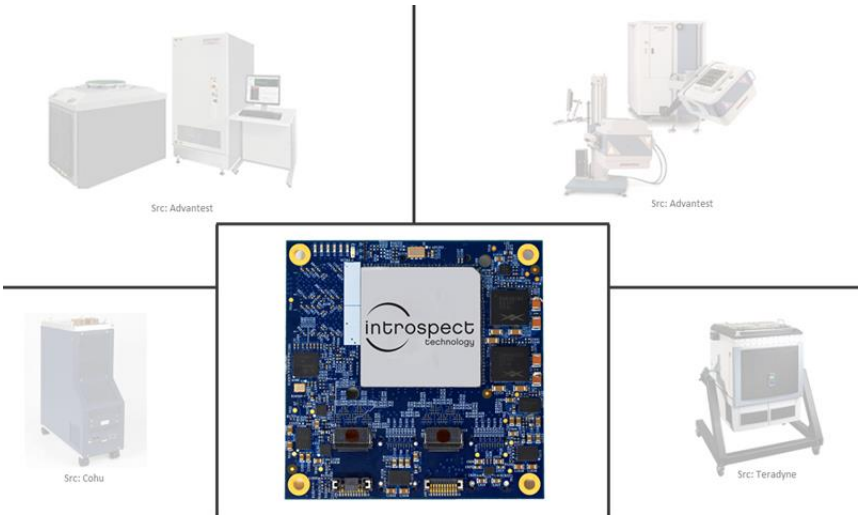
introspect technology

WHITE PAPER

MIPI Testing on Any ATE



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Introduction

The latest trend for semiconductor device manufacturers is to add several high-speed MIPI® Alliance ports to a single device. This enables feature-rich implementations of imaging-intensive and display-intensive applications, although it poses significant challenges for production test engineers who are tasked with creating high fault coverage testing solutions on ATE. Such fault coverage often entails creating a parallel, at-speed, system-oriented functional test while simultaneously grappling with the limitations of legacy ATE and the complexity of the MIPI protocols being tested.

In this paper, we describe production testing methodologies of MIPI-based devices on any ATE platform, whether this is at the wafer test stage or the final test stage. We first introduce the device classes that typically incorporate MIPI interfaces and some of the test methodology options that are available for test engineers. Subsequently, we identify the specific MIPI challenges for ATE testing and describe the Introspect Technology innovations that address them. We then present real-life case studies illustrating the major improvement in test execution efficiency and cost that have been achieved by large manufacturers deploying the Introspect SV4D Direct Attach MIPI Test Module on their ATE.

TYPICAL DEVICE CLASSES

Figure 1 shows different device classes that typically contain one or more MIPI ports. In Figure 1(a), a microcontroller or an applications processor is shown. This is typically the most complicated MIPI-based device, being able to process multiple camera (CSI-2℠) and display streams (DSI-2℠). Naturally, camera streams are usually input ports on an applications processor, and display streams are usually output ports. On the other hand, Figure 1(b) shows an image signal processor (ISP), in which there are both input and output camera streams. Similarly individual peripheral devices such as sensors and display driver ICs are shown (Figure 1(c)) as well as the all-important class of serializer and deserializer chips often found in automotive applications (Figure 1(d)).

Common to all device classes is a rapid increase in MIPI interface speed to a point that exceeds ATE capabilities. For example, at 10 Gbps aggregate

bandwidth, a conventional ATE system cannot generate the necessary signals to stimulate the high-speed interfaces nor analyze the received protocol data.

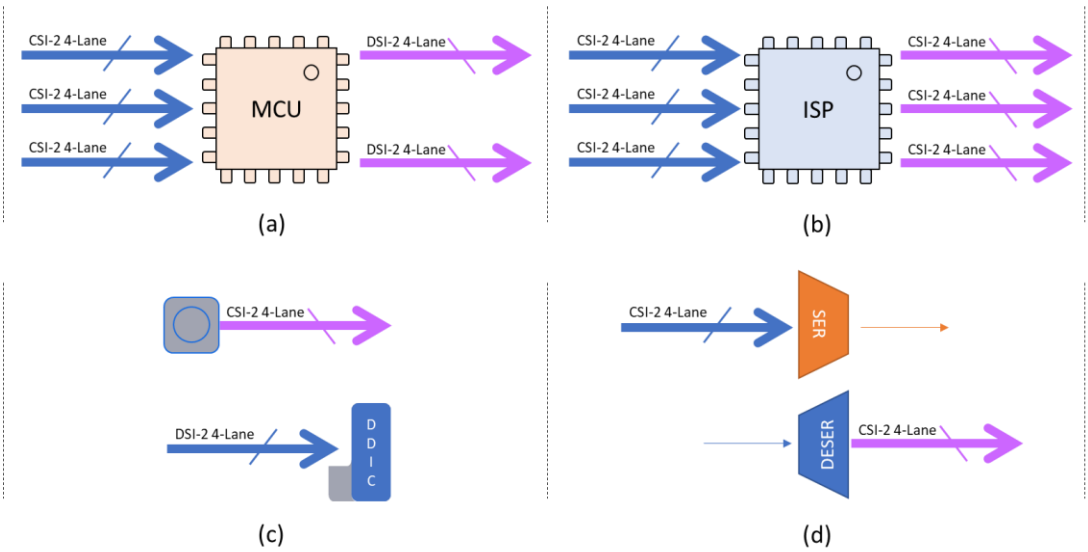

Figure 1: Different device classes containing MIPI interfaces

TEST METHODOLOGY SPECTRUM

Figure 2 illustrates the range of solutions available to production test engineers trying to create high-volume MIPI testing solutions on ATE. At the far left, an expensive ATE platform with very high-end channel cards can be used. However, as will be described shortly, the multi-mode, multi-level nature of MIPI signals means that various switching solutions need to be added in order to augment the ATE platform, therefore increasing test costs. Additionally, with MIPI being a *short-reach* interface, routing test signals between the device under test (DUT) and the ATE channel card is very challenging because the routing distance often creates a non-conformant condition for the DUT.

At the other end of the spectrum, golden devices can be placed on an ATE load board to perform simple go/no-go testing for the MIPI interface. While golden devices offer a cheaper alternative to high-end ATE instrumentation, they do not

offer *calibration* capability nor *instrument-grade* measurement. The Introspect Technology SV4D Direct Attach MIPI Test Module provides the best of both testing methodologies, sitting close to the DUT on an ATE load board while still offering calibrated and third-party supported test capability.

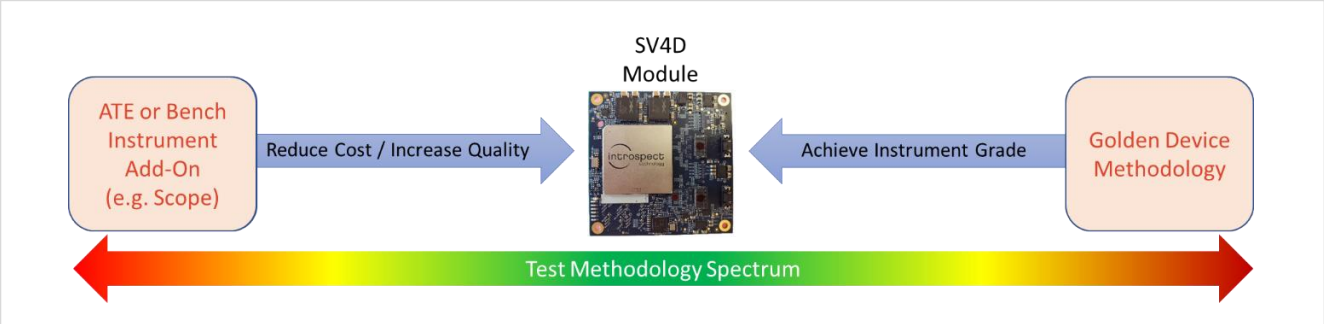

Figure 2: Production test methodology spectrum for MIPI-based devices

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In the next section, we describe the hardware requirements for enabling MIPI production test. Then, we proceed to describe the protocol requirements. Finally, we present three case studies on how the SV4D Direct Attach MIPI Test Module has been used to address both the hardware challenges and protocol challenges for different device class types.

Hardware Requirements for MIPI Testing

LP AND HS SIGNALING

One of the main hallmarks of the MIPI interface is the incorporation of both low-power and high-speed drivers on the same set of wires. The low-power drivers need to operate at LVCMOS levels (e.g. 1.2 V), they need to drive a high-impedance (Hi-Z) load, and they need to exhibit a controlled slew rate. On the other hand, the high-speed drivers operate at extremely low voltage levels and at speeds of up to 4.5 Gbps per lane. Referring to Figure 3, one can imagine the significant challenges associated with mimicking the MIPI dual-mode drivers on ATE. For one, the high-speed drivers are expected to operate at extremely high bandwidth while producing tiny voltage levels. Additionally, the transition between the low-power mode (signified by the blue waveform in the figure) and the high-speed mode (signified by the orange waveform) is extremely critical to achieving proper functional coverage for MIPI-based devices.

To create MIPI signals on a legacy ATE, the conventional method involves designing switch matrices on the load board in which two independent ATE channel cards are combined together to create the two MIPI signaling modes. Not only does this method end up costing more because two ATE channels must be consumed for each MIPI wire, but the task of designing this setup is cumbersome. Without getting into too much detail, there is the hardware design task of selecting switches and support components, the software design task of designing ATE vector files for each of the blue and orange waveforms in Figure 3 separately, and the system design task of understanding the nuances of the MIPI protocol timings. All of these activities represent a burden on test engineers and do not add immediate value to the task at hand, which is to achieve fault coverage for their own DUT. Most importantly, the resulting implementations often have serious signal integrity issues that jeopardize the quality of the test, and this is best illustrated in Figure 4. In this figure, the right-hand side panel shows typical waveforms that are achieved with conventional solutions. On the other hand, the figure shows (on the left) waveforms that are produced by a fully monolithic MIPI driver such as that found in the Introspect Technology SV4D Direct Attach MIPI Test Module.

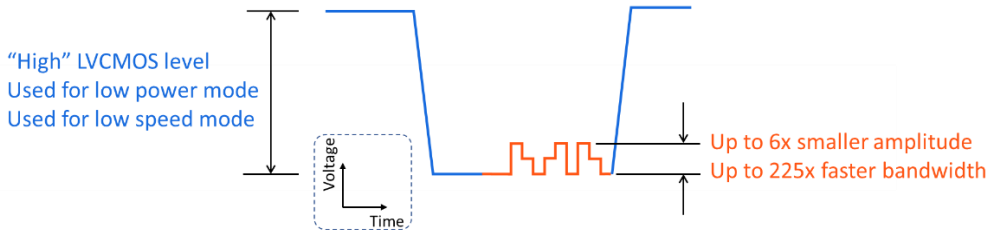

Figure 3: Illustration of the MIPI LP and HS signaling levels and speeds

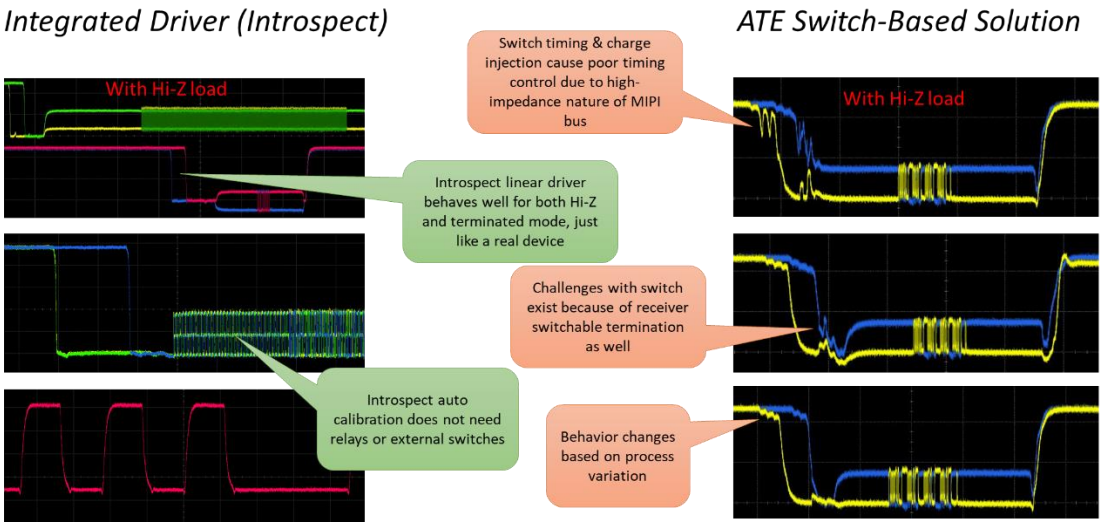

Figure 4: Benefits of an integrated driver (left panel) over a conventional ATE channel card with external switches (right panel)

MULTI-LEVEL HS DRIVERS AND RECEIVERS

Even within the high-speed mode of operation, a new trend in MIPI specifications is to rely on multi-level signaling. This is similar to the trend of deploying, say, PAM4 signaling on Ethernet communications buses. Figure 5 shows the block diagram of the physical layer driver within the Introspect Technology test modules, showing both a high-speed path with back-termination resistors and a low-speed path. The high-speed path is able to generate multi-level signals possessing high bandwidth, examples of which are shown in Figure 6.

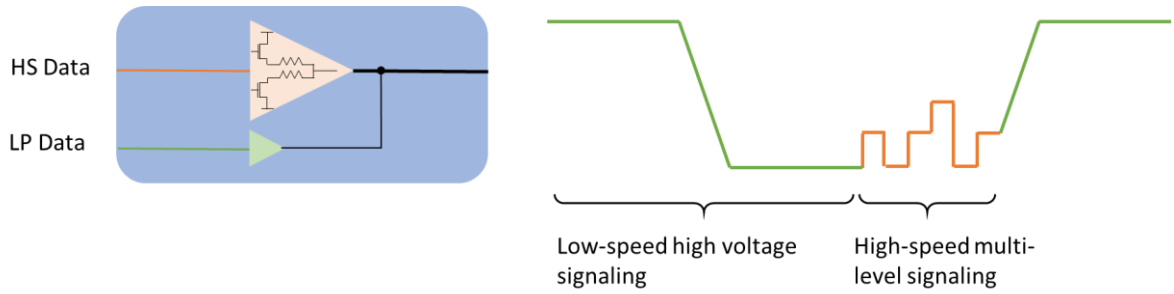

Figure 5: Block diagram of native MIPI physical layer drivers within the SV4D

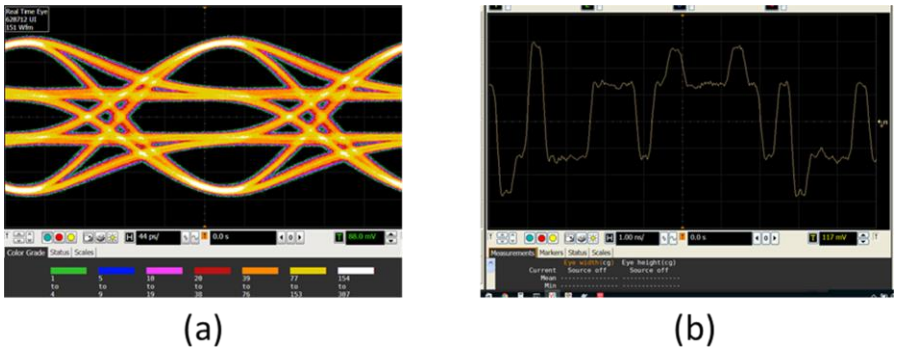

Figure 6: Advanced signal shapes in the SV4D module: (a) pre-emphasis eye diagram, (b) 4-level waveform

BIDIRECTIONAL BUS CONTROL

Certain MIPI devices rely heavily on a feature called Bus Turnaround (BTA), which is the MIPI Alliance's specification for performing half-duplex communications on a single bidirectional bus. For example, display driver ICs are programmed and operated almost entirely using this bidirectional communications method. Intended to limit pin count and maximize communications efficiency, the BTA feature requires a very rapid handshake between a master device and a slave device, a handshake in which the master can momentarily relinquish control of a bus and then take it back after the slave completes transmitting its data. A timing diagram of this handshake is shown in Figure 7(b), whereas Figure 7(a) shows the circuit diagram of the MIPI driver with the additional BTA receiver. In Figure 7(b), the highlighted pink segment is a time interval during which there is a potential overlap period with both sides of the bus attempting to drive the voltage on the wire. It is this overlap period that must be well understood in order to create a proper system-level test solution.

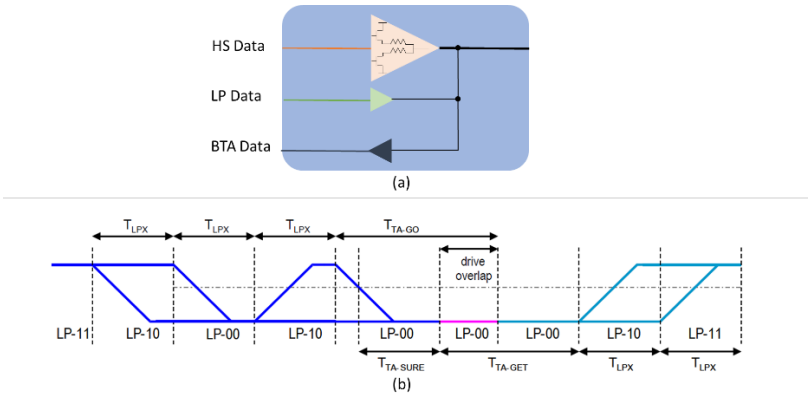

Figure 7: Bidirectional driver circuitry and timing diagram

Figure 8: Bus turnaround waveform from an actual device test sequence

Because the BTA handshake happens in a short time (equal to about one clock period of the signal being sent), any test instrument that performs BTA needs to be physically close to the DUT. Additionally, if a switch-based solution is implemented on the ATE load board, special care needs to be taken in order to understand the switch control latencies and whether they have any impact on the BTA response time as mentioned above. In the case of the Introspect Technology SV4D Direct Attach MIPI Test Module, its unique monolithic physical layer handles BTA responses natively. An example of a real device test containing the three phases of a BTA sequence is illustrated in Figure 8. On the left-hand side of the figure, the SV4D is shown driving a BTA request command. Then, as time progresses, the DUT takes over the bus and responds with its data, and finally, the SV4D takes back control of the bus. This entire sequence is performed autonomously within the SV4D.

Protocol Requirements for MIPI Testing

PACKET BASED COMMUNICATION

All MIPI protocols rely on a packet-based transmission system. This means that vectors containing functional test data need to also be able to cover all the protocol overhead elements that are required for an error-free transmission. For example, all packets must have proper headers, proper ECC values, and proper CRC fields. These concepts are illustrated briefly in Figure 9. Functionally testing a device means that the elements shown in the figure have to be programmed, and this is achieved easily using the Introspect SV4D's programming API. On the other hand, if a conventional bit-by-bit ATE vector is used, then significant effort has to be undertaken to slowly build up the protocol, and this is a very error-prone activity.

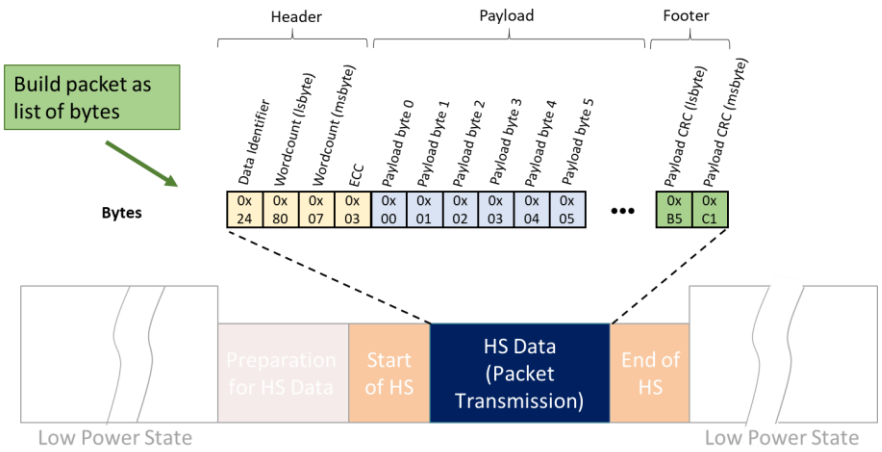

Figure 9: Packet-based transmissions in MIPI

DEVICE CONTROL THROUGH THE MIPI INTERFACE

As mentioned previously, many devices rely completely on the MIPI interface for device initialization and programming. This means that even test modes must be

entered programmatically through the protocol and not through some side-band mechanism such as JTAG. The result is increasing test development complexity. If a complete protocol sequence is required to start up a device, then the best solution for this task is to use an instrument that is completely protocol-aware and that has a complete MIPI programming API. Indeed, it is this protocol-based device control that was a major motivator for the development of the SV4D Direct Attach MIPI Test Module. Referring to Figure 10, the SV4D can simply be programmed to perform register write/read operations on a device under test in order to initialize it. The figure shows a zoomed-out timing trace (top two panels) of many register transfers between the SV4D and the DUT before an image frame is sent to the latter for testing it (the bottom trace of the figure is a zoom into one of the register commands).

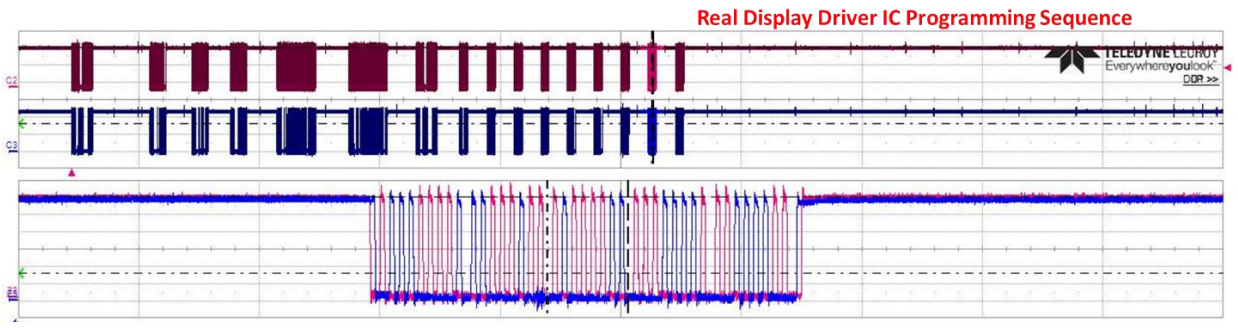

Figure 10: Programming sequence for initializing a display driver IC

FUNCTIONAL TESTING

Building up on the previous two sections, this section shows a concrete example of the importance of protocol-based testing in MIPI. In Figure 11, a functional programming sequence is shown using two methods: the Introspect Technology MIPI programming API in the left panel and a conventional vector file in the right panel. As can be seen, the left panel represents a high-level method for functionally exercising a device, exactly the way it is intended to be used in its final application. On the other hand, the conventional vector file is extremely cumbersome to use. Indeed, the difficulty in using ATE vector files often forces

many test engineers to compromise on test functionality and hence fault coverage. This lack of fault coverage was another major motivator for developing the SV4D and its associated software tools.

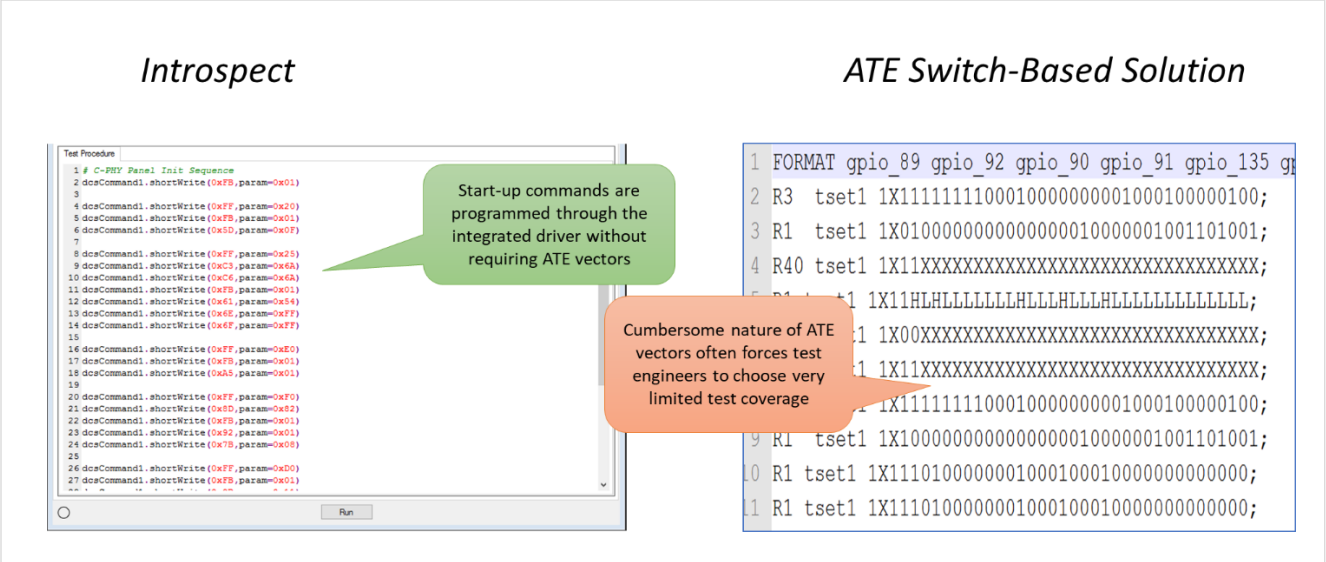

Figure 11: Benefits of a complete MIPI programming API (left panel) over a conventional ATE vector file (right panel)

Case Studies

MICROCONTROLLER CSI-2 RECEIVER TEST ON A LEGACY ATE

In this section, we highlight a microcontroller test application in which device pass/fail checking is performed using a side-band method. Referring to Figure 12, a single SV4D port is used to drive MIPI CSI-2 traffic over a D-PHY℠ bus connected to the DUT. The SV4D itself is controlled by the ATE using a master-slave arrangement in which the ATE is the master, sending simple register commands to the SV4D, and the SV4D is the slave. When the ATE instructs the SV4D to transmit high-speed MIPI data to the DUT (step 1 in the figure), the SV4D responds by performing the transmission (step 2 in the figure), and then the DUT status is checked independently using either the ATE or the SV4D itself (step 3 in the figure). Critical to all of this is that a single, slow timing cycle is needed on the ATE side since all the high-speed operations are performed within the SV4D. A timing diagram of this test flow is shown in Figure 13.

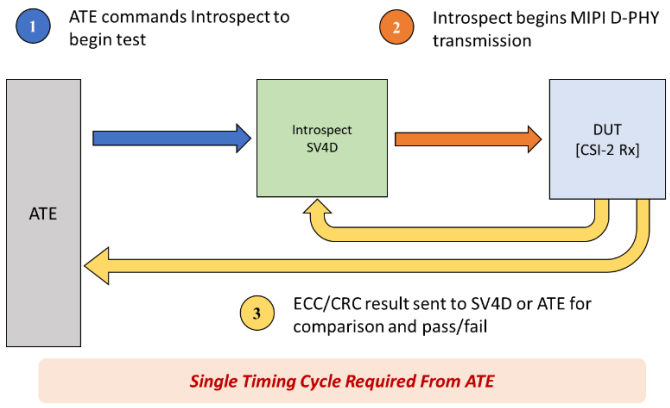

Figure 12: Microcontroller test setup with side-band response checking. ATE frequency is ~10 MHz

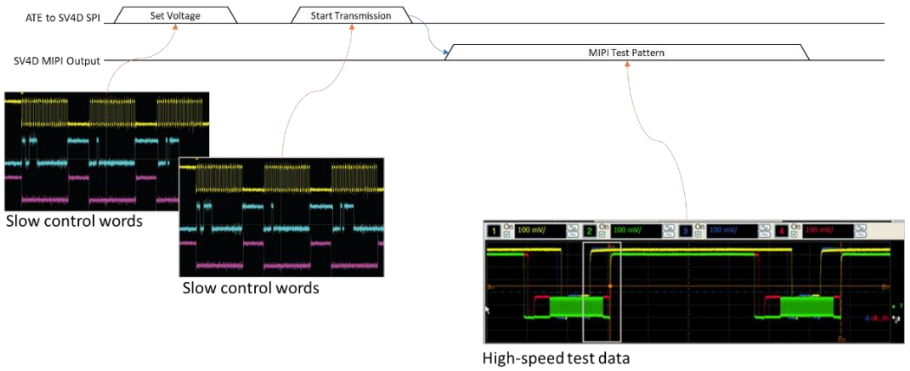

Figure 13: Timing diagram of the microcontroller CSI-2 receiver test

DISPLAY DRIVER IC TEST WITH INTEGRATED DEVICE RESPONSE CHECKING

In this application, we note that all DUT response checking is performed entirely over the MIPI bus. Thus, the load board design was quite simple, and most of the sophistication existed within the SV4D and its corresponding software API. Referring to Figure 14, the test procedure consisted of starting up the device over MIPI (as shown in previous sections), then transmitting video data at high speed (first two bursts in the figure), then performing a BTA request to check if the video has been received without any CRC errors. That is, the DSI-2 protocol within the DUT had been enabled through the initialization sequence to start its CRC error counters. Then, after at-speed video data is transmitted from the SV4D to the DUT, a simple BTA command is issued. Depending on whether the DUT experienced a transmission error or not, it responds with an Acknowledge or an Acknowledge and Error Report. As can be seen, the protocol-aware nature of the SV4D enables short, yet sophisticated test sequences in this case study.

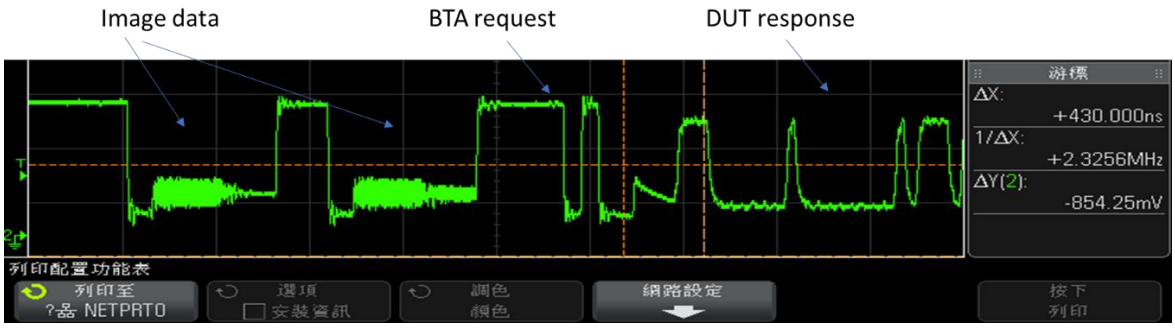

Figure 14: DDIC case study in which device pass/fail checking happened through BTA after image transmission

IMAGE SENSOR TEST USING LEGACY IMAGE PROCESSING SOFTWARE

It is often desirable to reuse image processing algorithms from legacy ATE implementations, especially in the context of image sensor test applications. To enable this while still offering the ability to capture sensor data at high speed over the MIPI interface, the SV4D can be configured as a serial-to-parallel converter or bridge device. In this mode, the SV4D contains a complete functional CSI-2 receiver for pixel extraction and frame reconstruction. Then, instead of performing internal pass/fail testing on the reconstructed frame, the SV4D re-transmits in real-time (or "streams") the received pixel data out over a parallel bus running at speeds that are compatible with the legacy ATE. This parallel bus feeds directly into the legacy ATE and allows for reusing any existing signal processing algorithms. An illustration of this test application is shown in Figure 15. The SV4D contains up to 40 single-ended or 20 differential parallel drivers for this application.

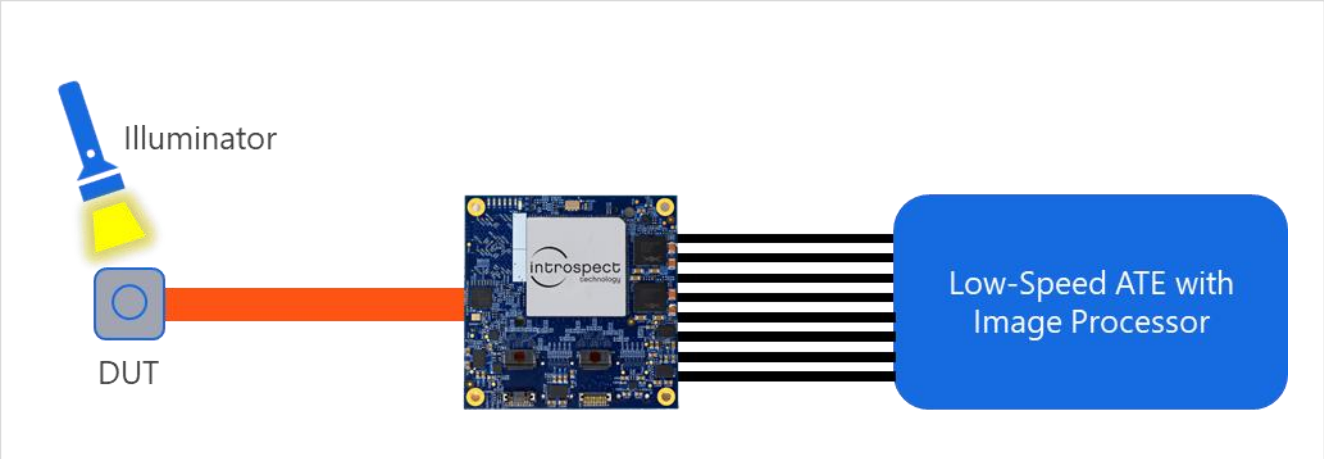

Figure 15: Image sensor test application in which the SV4D acts as a serial to parallel converter

Conclusion

This paper described testing MIPI device interfaces on any ATE. We introduced the hardware and protocol requirements for achieving a reliable test methodology for state-of-the-art MIPI-based devices, and we introduced how the Introspect Technology SV4D Direct Attach MIPI Test Module addresses these requirements with tremendous ease. The SV4D was shown to have world-class hardware features including a monolithic physical layer capable of operating in both a low-power and a high-speed signaling mode and capable of performing autonomous BTA communications. It was also shown to possess a strong MIPI programming API, thus greatly simplifying the test development process for functional test applications. Additionally, the SV4D's native protocol reception and transmission features were introduced for applications such as image sensor testing. Finally, three separate case studies were presented, each highlighting the different requirements that were presented earlier and how they are addressed by the SV4D. Most notably, it was shown how the SV4D helped major device manufacturers improve test coverage and reduce test cost without requiring heavy investment in high-end ATE platforms.

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1.0	Document Release	June 20, 2019

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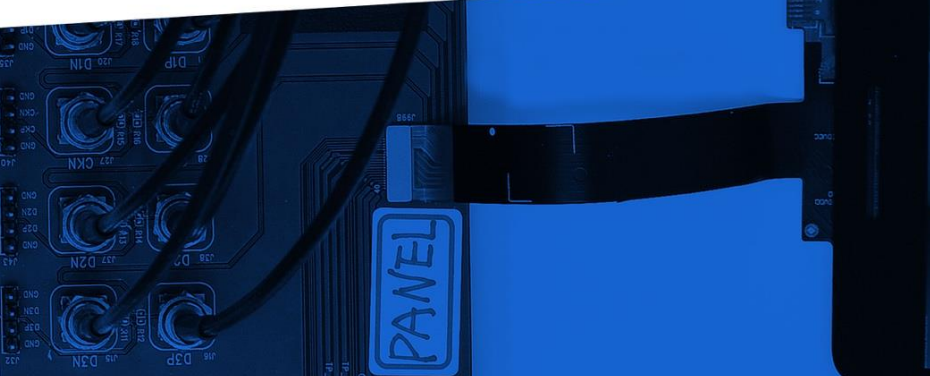

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