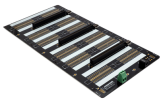
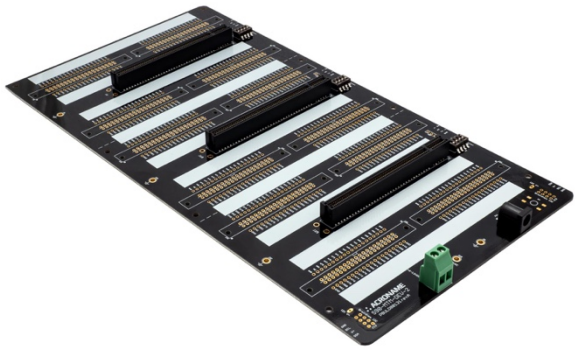




Overview

The Acroname MTM Development Board 2.0 (S90-MTM-DEV-2), part of Acroname® MTM (Manufacturing Test Module) product series, is a connectivity solution designed for development or integration to wire-based testers. The MTM-DEV-2 allows MTM system designers to easily and quickly access MTM module resources through direct soldering, 0.1" headers or ribbon cable connections.

Ideal for use in high-reliability manufacturing or development testing environments, MTM-DEV-2 includes three policy-free slots, allowing access to up to three MTM modules installed in any combination.

Based on Acroname's industry-proven and well-adopted BrainStem® technology, resources on MTM modules installed in the MTM-DEV-2 are controlled and accessed via Acroname's powerful and extensible BrainStem software APIs.

Typical Application

- Manufacturing functional testing
- Validation testing
- Automated test development
- Embedded system development

System Features

- 3 policy-free MTM module slots
- BrainStem network connection between slots
- DIP switches to customize BrainStem addresses
- 6-12V power input via barrel jack or screw terminal connection
- BrainStem bus connection for expansion
- Pin access to MTM resources on all MTM slots
- Customizable to support direct wire soldering, ribbon cable or terminal style connectors

Description

The MTM-DEV-2 breakout board is a convenient component for manufacturing test solutions implementing MTM using wired connections. Details on the MTM development platform architecture, BrainStem interface, and APIs are at https://acroname.com/reference.

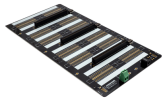
The MTM-DEV-2 implements three (3) policy-free MTM slots to accommodate any three MTM modules in any combination.

The high-density connections of the MTM modules are broken out to low-density 0.1" spaced connections. Headers, screw terminals or ribbon cable connectors can be installed to customize the connectivity needed in a given test system.

Modules installed in MTM-DEV-2 are networked together via a local I2C-based BrainStem network. DIP switches near each slot allow custom addressing of each module on the BrainStem network. Two optional connectors on MTM-DEV-2 allow the BrainStem network to be expanded to other BrainStem enabled devices or development boards. Features of any MTM modules installed are easily controlled via the BrainStem API.

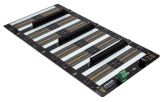
Within the MTM platform architecture, any MTM module can operate either independently or as a component in a larger network of MTM modules. Each module is uniquely addressable and controllable from a host by connecting via the on-board USB connection, the module's card-edge USB input or through other MTM modules on the local MTM/BrainStem I2C bus.

IMPORTANT NOTE:
The MTM-DEV-2, utilizes a PCIe connector interface but is for use strictly in MTM-based systems. It should never be installed in a PCI slot of a host computer directly. Insertion into a PC or non-MTM system could cause damage to the PC.



Absolute Maximum Ratings

Any ABSOLUTE MAXIMUM RATINGS for MTM-DEV-2 will be specific to the MTM modules installed. Please refer to the datasheets related to specific MTM modules for the relevant ABSOLUTE MAXUMUM RATINGS.



Block Diagram

Showing populated and not populated (NP) connectors:

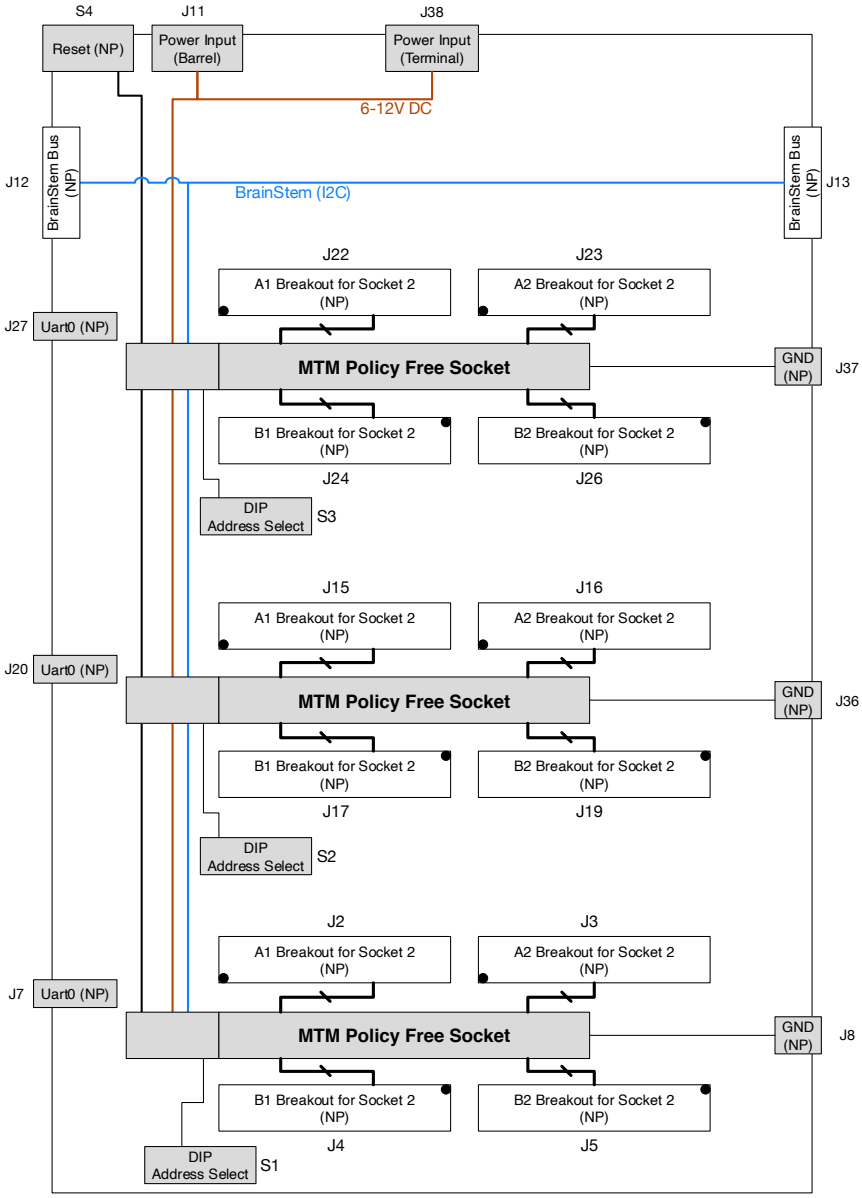
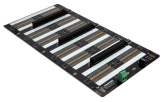


Figure 1: MTM-DEV-2 Block Diagram



Typical Applications

Automated Functional Circuit Test (FCT) using MTM to wire-wrapped test point pogos:

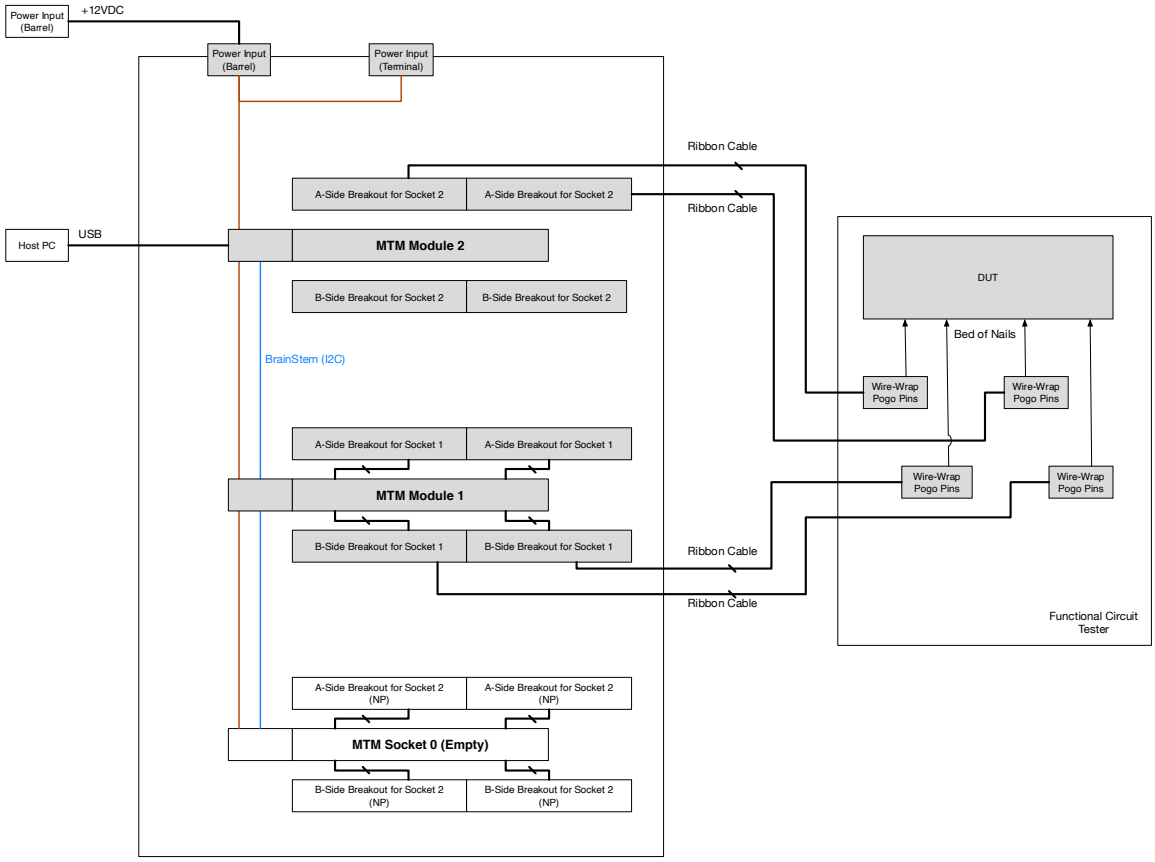
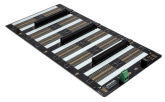


Figure 2: Typical Automated Functional Tester Application



Connector List

List of connectors on MTM-DEV-2:

Connector Designator	Description	Pins	Populated
J1	MTM Module Socket 0	164	Yes
J2	MTM Socket 0: A-side breakout A1	40	No
J3	MTM Socket 0: A-side breakout A2	40	No
J4	MTM Socket 0: B-side breakout B1	40	No
J5	MTM Socket 0: B-side breakout B2	40	No
J7	MTM Socket 0: UART0	4	No
J11	Barrel Power Input	3 (2pin Barrel)	Yes
J12	BrainStem Bus Expansion	8	No
J13	BrainStem Bus Expansion	8	No
J14	MTM Module Socket 1	164	Yes
J15	MTM Socket 1: A-side breakout A1	40	No
J16	MTM Socket 1: A-side breakout A2	40	No
J17	MTM Socket 1: B-side breakout B1	40	No
J19	MTM Socket 1: B-side breakout B2	40	No
J20	MTM Socket 1: UART0	4	No
J21	MTM Module Socket 2	164	Yes
J22	MTM Socket 2: A-side breakout A1	40	No
J23	MTM Socket 2: A-side breakout A2	40	No
J24	MTM Socket 2: B-side breakout B1	40	No
J26	MTM Socket 2: B-side breakout B2	40	No
J27	MTM Socket 2: UART0	4	No
J38	Terminal Power Input	2	Yes

Table 1: MTM-DEV-2 Connectors

Pinout Descriptions

WARNING: Acroname's MTM line features a PCIe connector that is common in most desktop computers; however, they are NOT intended nor designed to work in these devices. Do NOT insert this product into any PCIe slot that wasn't specifically designed for this product! Failure to follow this warning WILL result in damage to this product and any device you connect it to.
The MTM edge connector A side and B side pins are shown in the following diagram. The A and B side pins common to all of the modules are listed in table 2. The S90-MTM-DEV-2 board includes 3 identical policy free slots. Figure 4 shows the common pinout for each socket.

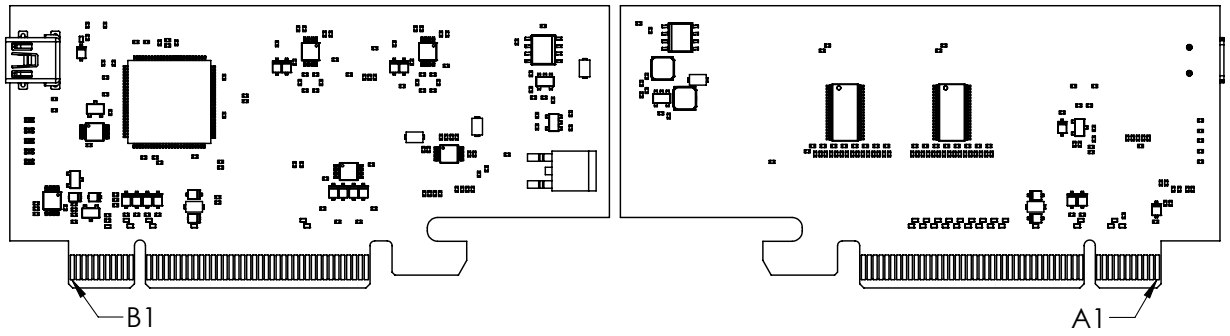


Figure 3: MTM A/B Sides

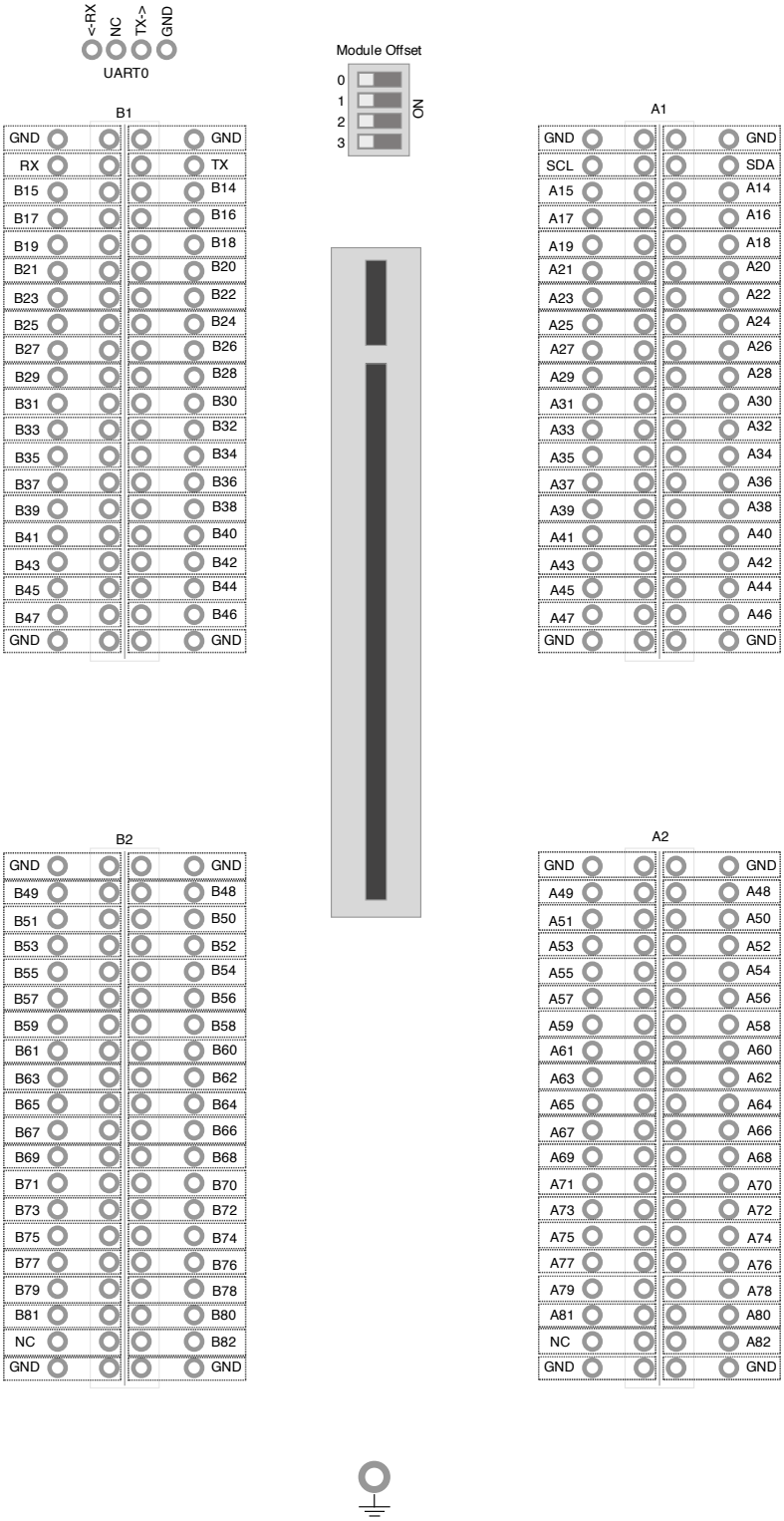
J1, J14, J21: MTM Socket Common Pins

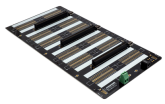
Edge Connector Side A	Edge Connector Side A Description	Breakout A1	Edge Connector Side B	Edge Connector Side B Description	Breakout B1
A1	GND	1	B1	Input Voltage, V_{supply}	-
A2	GND	2	B2	Input Voltage, V_{supply}	-
A3	GND	-	B3	Input Voltage, V_{supply}	-
A4	GND	-	B4	Input Voltage, V_{supply}	-
A5	Reset[2]	All MTM, RST Button	B5	Input Voltage, V_{supply}	-
A6	GND	-	B6	Reserved, Do Not Connect	-
A7	GND	-	B7	Reserved, Do Not Connect	-
A8	I²C0 SCL[1]	3	B8	GND	-
A9	I²C0 SDA[1]	4	B9	GND	-
A10	GND	-	B10	Reserved, Do Not Connect	-
A11	GND	-	B11	Reserved, Do Not Connect	-
A12	Module Address Offset 0	MTM SW0	B12	Module Address Offset 2	MTM SW2
A13	Module Address Offset 1	MTM SW1	B13	Module Address Offset 3	MTM SW3

Table 2: MTM Common pins

[1] I²C0 SCL and SDA nets are connected to all MTM module sockets and the BrainStem bus connectors (not populated)
[2] Reset net is connected to all MTM module sockets and the reset push button (not populated)

Policy Free Socket Pinout (J6, J18, J25)



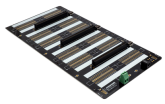


A1 Pins (J2, j15, j22)

Pin	Description
GND	GND
SCL	i2C1 Clock
SDA	i2C1 Data
A15	Module Specific
A16	Module Specific
A17	Module Specific
A18	Module Specific
A19	Module Specific
A20	Module Specific
A21	Module Specific
A22	Module Specific
A23	Module Specific
A24	Module Specific
A25	Module Specific
A26	Module Specific
A27	Module Specific
A28	Module Specific
A29	Module Specific
A30	Module Specific
A31	Module Specific
A32	Module Specific
A33	Module Specific
A34	Module Specific
A35	Module Specific
A36	Module Specific
A37	Module Specific
A38	Module Specific
A39	Module Specific
A40	Module Specific
A41	Module Specific
A42	Module Specific
A43	Module Specific
A44	Module Specific
A45	Module Specific
A46	Module Specific
A47	Module Specific

A2 Pins (J3, j16, j23)

Pin	Description
GND	GND
A48	Module Specific
A49	Module Specific
A50	Module Specific
A51	Module Specific
A52	Module Specific
A53	Module Specific
A54	Module Specific
A55	Module Specific
A56	Module Specific
A57	Module Specific
A58	Module Specific
A59	Module Specific
A60	Module Specific
A61	Module Specific
A62	Module Specific
A63	Module Specific
A64	Module Specific
A65	Module Specific
A66	Module Specific
A67	Module Specific
A68	Module Specific
A69	Module Specific
A70	Module Specific
A71	Module Specific
A72	Module Specific
A73	Module Specific
A74	Module Specific
A75	Module Specific
A76	Module Specific
A77	Module Specific
A78	Module Specific
A79	Module Specific
A80	Module Specific
A81	Module Specific
A82	Module Specific



B1 Pins (J4, j17, j24)

Pin	Description
GND	GND
RX	Uart0 RX
TX	UART0 TX
B15	Module Specific
B16	Module Specific
B17	Module Specific
B18	Module Specific
B19	Module Specific
B20	Module Specific
B21	Module Specific
B22	Module Specific
B23	Module Specific
B24	Module Specific
B25	Module Specific
B26	Module Specific
B27	Module Specific
B28	Module Specific
B29	Module Specific
B30	Module Specific
B31	Module Specific
B32	Module Specific
B33	Module Specific
B34	Module Specific
B35	Module Specific
B36	Module Specific
B37	Module Specific
B38	Module Specific
B39	Module Specific
B40	Module Specific
B41	Module Specific
B42	Module Specific
B43	Module Specific
B44	Module Specific
B45	Module Specific
B46	Module Specific
B47	Module Specific

B2 Pins (J5, j19, j26)

Pin	Description
GND	GND
B48	Module Specific
B49	Module Specific
B50	Module Specific
B51	Module Specific
B52	Module Specific
B53	Module Specific
B54	Module Specific
B55	Module Specific
B56	Module Specific
B57	Module Specific
B58	Module Specific
B59	Module Specific
B60	Module Specific
B61	Module Specific
B62	Module Specific
B63	Module Specific
B64	Module Specific
B65	Module Specific
B66	Module Specific
B67	Module Specific
B68	Module Specific
B69	Module Specific
B70	Module Specific
B71	Module Specific
B72	Module Specific
B73	Module Specific
B74	Module Specific
B75	Module Specific
B76	Module Specific
B77	Module Specific
B78	Module Specific
B79	Module Specific
B80	Module Specific
B81	Module Specific
B82	Module Specific

J11 2-pin Barrel: Power

Pin	Description
1	Center / Vsupply
2	Ring / GND
3	Ring / GND

Table 2: Pinout for Barrel Power Connector

J38 2-pin Terminal: Power

Pin	Description
1	Vsupply
2	GND

Table 3: Pinout for Terminal Power Connector

J12, J13: BrainStem I2C

Pin	Description
1	GND
2	GND
3	SCL
4	SCL
5	Reserved (I2C V+)
6	Reserved (I2C V+)
7	SDA
8	SDA

Table 4: Pinout for BrainStem I2C Connectors

J7, J20, J27: MTM Socket UART0

Pin	Description
1	GND
2	TX
3	NC
4	RX

Table 5: Pinout for MTM Socket UART Connectors

Module Connectivity

BrainStem:

Module slots on MTM-DEV-2 are connected together using the BrainStem bus through I2C0 on pins A8 and A9 of the PCIe edge connector. The BrainStem bus is accessible through J12 or J13 connectors for external access or expansion to other BrainStem enabled devices.

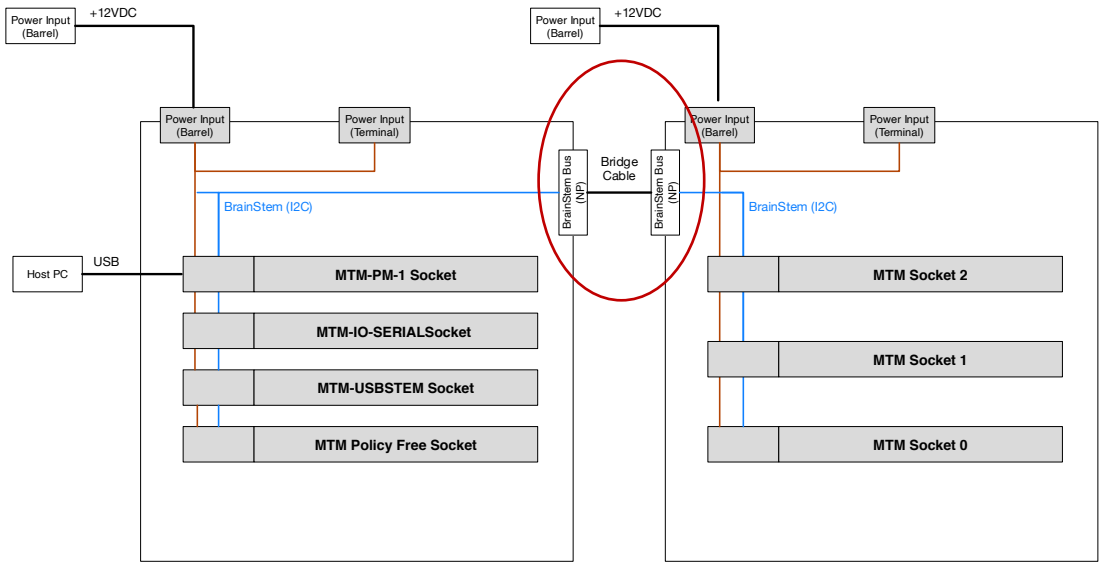
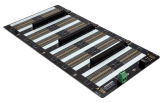


Figure 3: Bridging multiple MTM-DEV-2 boards using BrainStem



MTM Edge Connector Interface

All MTM products are designed with an edge connector interface that requires a compatible edgeboard connector on the carrier PCB. Acroname recommends the through-hole PCI-Express (PCIe) Vertical Connector. The connectors can be combined with an optional retention clip, as shown below. MTM-DEV-2 is populated with 164-position connectors which accept any MTM module.

Manufacturer	Manufacturer Part Number	Description
Amphenol FCI Samtec	10018784-10203TLF PCIE-164-02-F-D-TH	PCI-Express 164-position vertical connector
Amphenol FCI	10042618-003LF	PCI-Express Retention Clip (optional)

Table 6: PCI-Express Edge Connectors for MTM Products

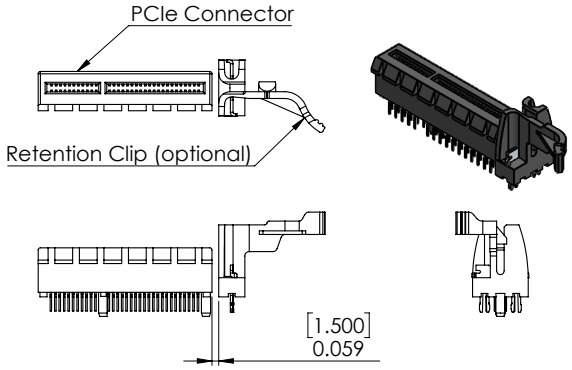


Figure 4: PCIe Vertical Connector with optional Retention Clip

MTM Edge Connector Specifications	Description
Contact Finish	Gold
Card Thickness	0.0625" [1.59mm]
Number of Rows	2
Number of Positions	Variable (see Table 6: PCI-Express Edge Connectors for MTM Products)
Pitch	0.039" (1.00mm)

Table 7: MTM Edge Connector Specifications

Breakout Connector Interface

Breakouts for MTM modules are provided on 0.1" spaced connectors. Though specific connectors are required, Acroname has designed MTM-DEV-2 to accommodate standard 0.1" pitch headers. Suggested connectors include:

Breakout Connector Specifications	Description
Contact Finish	Gold
Number of Rows	2
Number of Positions	Variable
Pitch	0.1" (2.54mm)

Table 8: Suggested Breakout Connectors

Mechanical

Dimensions are shown in mm. 3D CAD models are available through the MTM-DEV-2 product page Downloads section and from: https://a360.co/37HZWgM

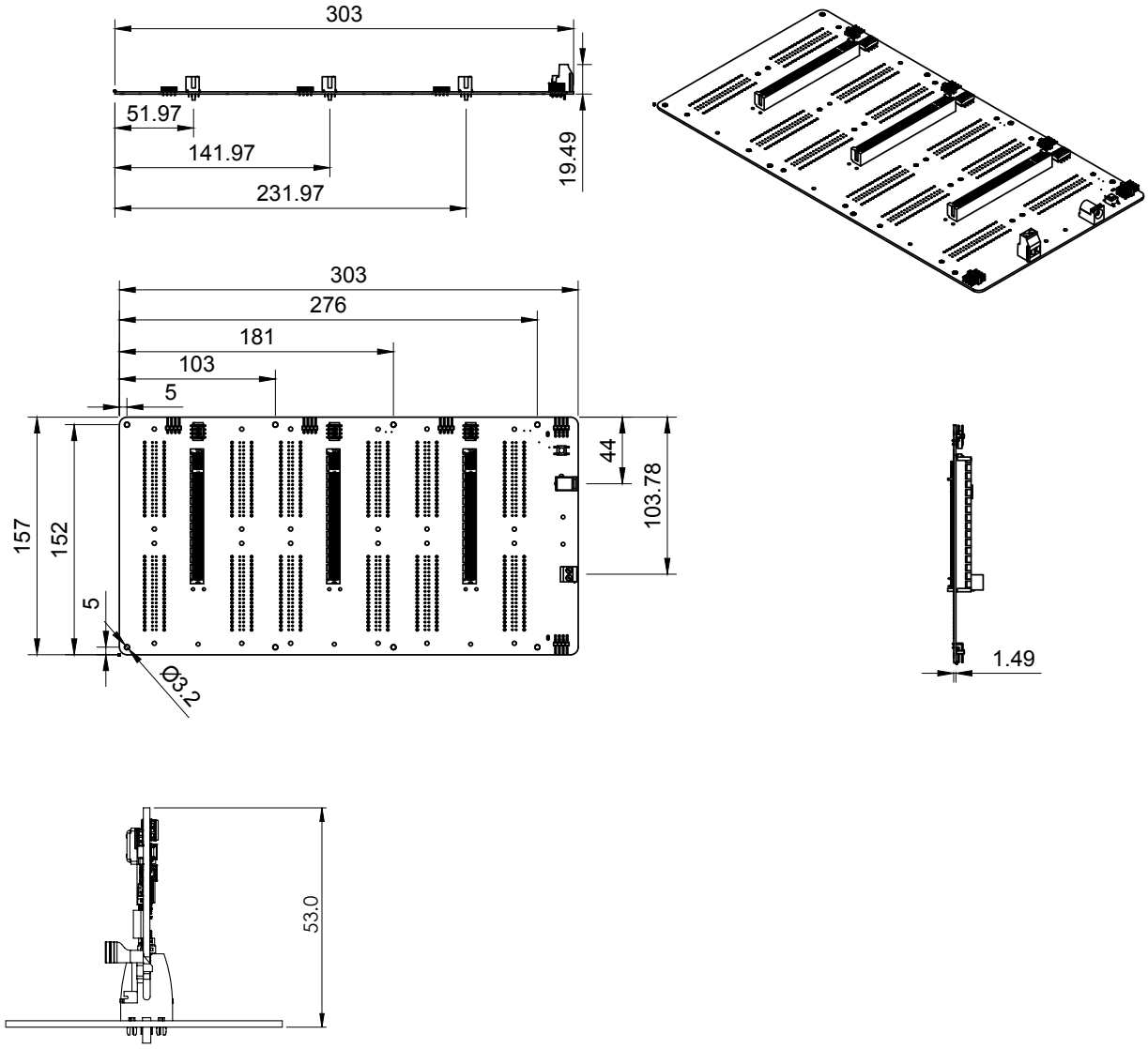


Figure 5: MTM-DEV-2 Mechanical

Module Address Hardware Offset Configuration

A hardware offset is one of two ways to modify the module's address on the BrainStem network. Using hardware offset pins is useful when more than one of the same type of module is installed on a single BrainStem network. Applying a different hardware offset to each module of the same type in one network allows for all the modules to seamlessly and automatically configure the network for inter-module communication. Further, modules can be simply swapped in and out of the network without needing to pre-configure a module's address before being added to a network. Finally, when a system has more than one of the same type of module in a network, the module address hardware offset can be used to determine the module's physical location and thus its interconnection and intended function. For detailed information on BrainStem networking see the BrainStem software reference at https://acroname.com/reference

Each hardware offset pin can be left floating or pulled to ground with a 1kΩ resistor or smaller (pin may be directly shorted to ground). Pin states are only read when the module boots, either from a power cycle, hardware reset, or software reset. The hardware offset pins are treated as a binary number which is multiplied by 2 and added the to the module's base address. The hardware offset calculation is detailed in the following table.

HW Offset Pin				Address Offset	Module Base Address	Final Module Address
3	2	1	0			
NC	NC	NC	NC	0	4	4
NC	NC	NC	1	2	4	6
NC	NC	1	NC	4	4	8
NC	1	NC	NC	8	4	12
1	NC	NC	NC	16	4	20
1	NC	NC	1	2+16	4	22

Table 9: Module address hardware offset examples

Document Revision History

All major documentation changes will be marked with a dated revision code

Revision	Date	Engineer	Description
1.0	June 15, 2018	LCD	Initial Release
1.1	July 2020	ACRO	Formatting, diagram updates