QUICK START GUIDE

Daisy Trigger Mode

Pattern Starts with Consistent Skew

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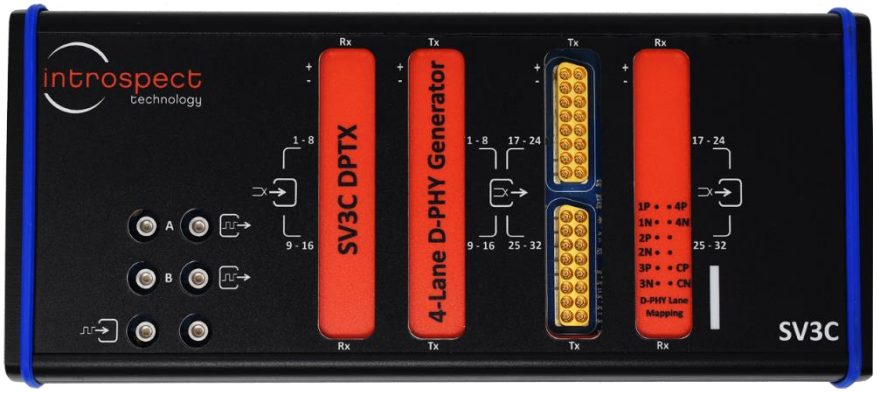

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Introduction

The SV3C-DPTX Generator introduces the daisy trigger mode which is used to trigger pattern starts across a daisy chain of modules with consistent skew across modules from one pattern start to the next, within a clock commit.

Setup

The head is the module that will receive a trigger from the DUT if a DUT is present. The head forwards the trigger to the slave via the 12-pin header.

1. Connect pin 1 of the head 1 to pin 6 of the slave.
2. Connect CLKOUTA of the head to CLKIN of the slave.
3. If DUT is present, connect trigger from DUT to pin 6 of the head.
4. Connect pin 4 of the head to pin 5 of the slave.
5. Connect pin 4 of the slave to pin 5 of the head.

HARDWARE CONNECTIONS FOR TWO DAISY-CHAINED SV3C DPTX/CPTX MODULES

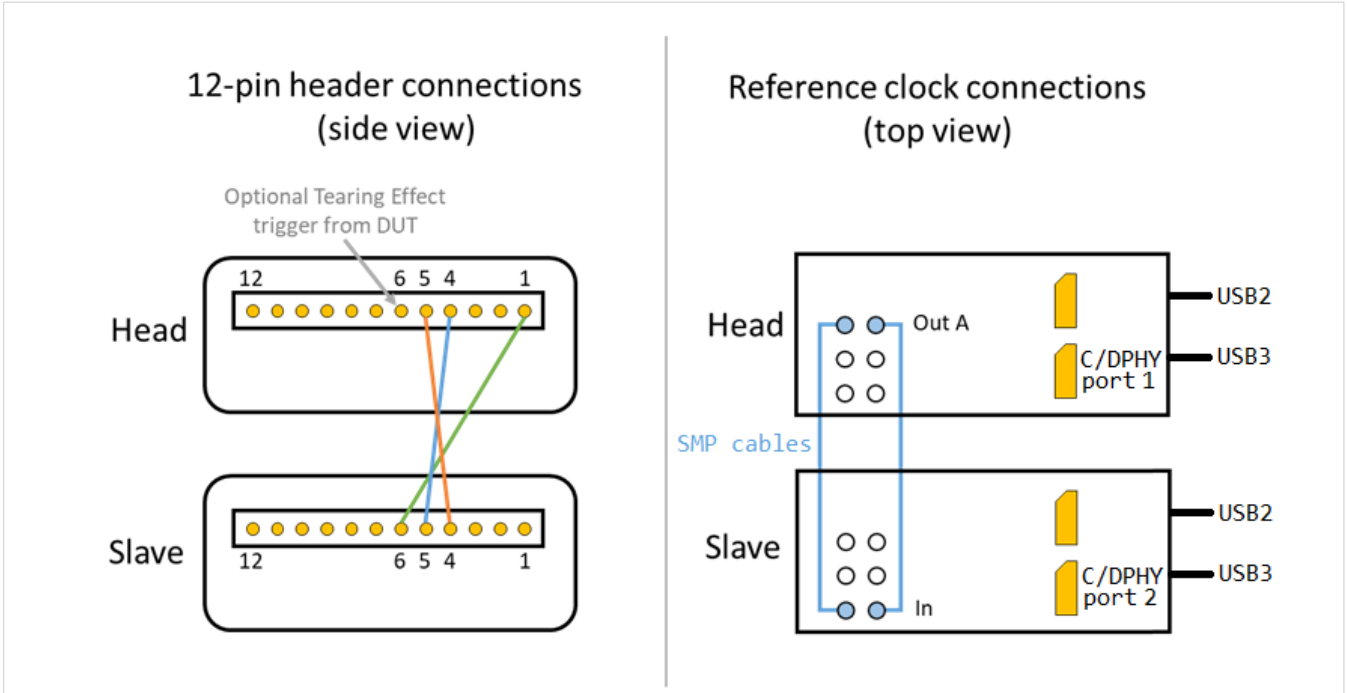

Figure 1: Diagram of the hardware connections.

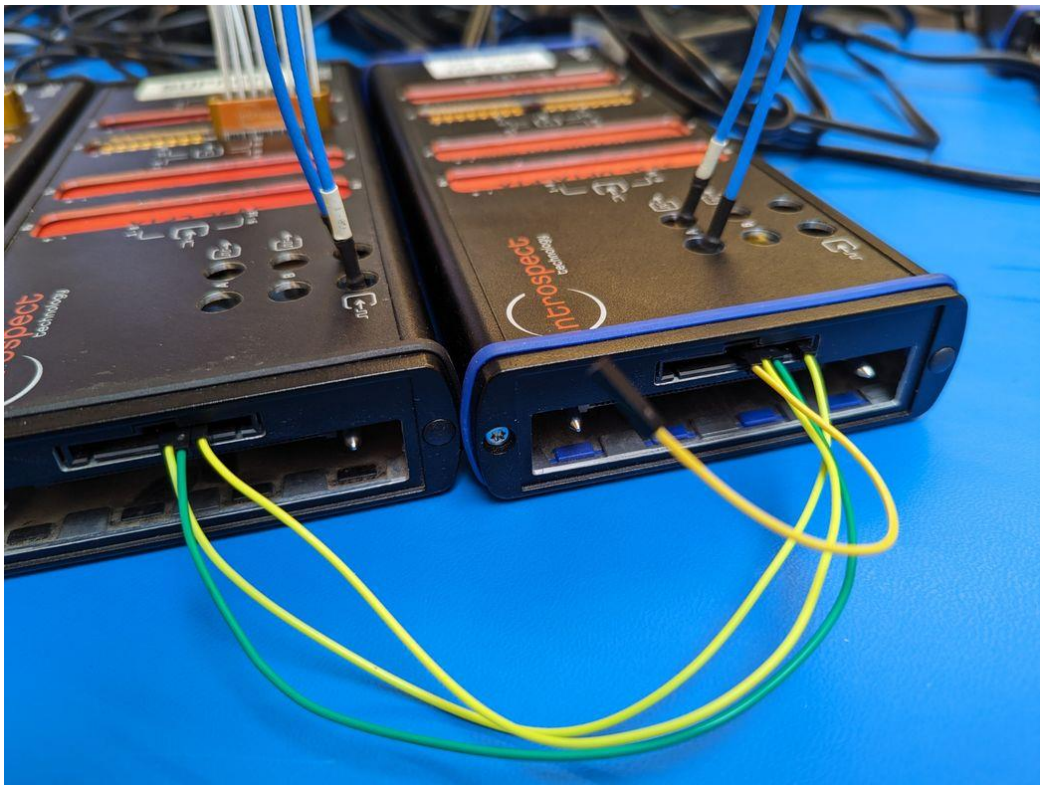

Figure 2: Photo of two daisy-chained modules.

Test Procedures

Once you have recreated the setup above, connect to each module (using separate SV3C_4L6G_MIPI_DPHY_GENERATOR IESP instances) using the following tests:

- Head test procedure: DphyTwoPortMaster
- Slave test procedure: DphyTwoPortSlave

1. Hit run on head test first, and then hit run on slave test.
2. Follow the dialog box flow below. The flow consists of an initialization step followed by an iteration for each pattern start.
   - The modules reset to LP11 after the "Reset patterns and wait for trigger" boxes.
   - The pattern starts on both modules after the "Send pattern start trigger" boxes.
   - The skew across modules is consistent for each pattern loop iteration during the test.

On the slave procedure, make sure you are using an external clock reference like this:

- mipiClockConfig1.referenceClocks = refClocksConfig1
- refClocksConfig1.sytemRefClockSource = external
- refClocksConfig1.externaRefClockFreq = 100.0

Rerunning the Tests

If you rerun the test procedures as is, this will redo the clock commit (mipiDphyGenerator1.setup) which will change the pattern skew. The skew (module 2 - module 1) across clock commits vary from about -40 ns to +80 ns.

REVISION NUMBER	HISTORY	DATE
1.0	Document Release	May 22, 2024

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