



WHITE PAPER

MIPI Testing in ADAS

SERIES NAME





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Table of Contents

Table of Contents	2
List of Figures	3
Introduction	4
FPD-Link	5
ADAS Sub-System	5
Test Scenarios	7
Scenario #1: Live Link Test	7
Scenario #2: Image Capture Test	9
Scenario #3: Image Generator Test	9
Test Execution & Results	10
Scenarios #1 & 2: DPHY Analyzer	10
Example1: Frame Capture	10
Analysis Results	12
Frame View	13
Example2: Burst Capture	13
Analysis Results	12
Burst With No Errors	15
Burst With Errors	16
Packet View	17
Frame View	18
Scenario #3: DPHY Generator	19
Conclusion	22





List of Figures

Auto SerDes links are used in ADAS systems to drive long cables (Source: MIPI Al	liance)
	4
FPD-Link III sub-system under test Block diagram	5
FPD-Link III sub-system under test (DUT)	6
Live Link Test Block Diagram	7
Photo of Live Link showing probe insertion at input of SBC	8
Image Capture Test Block Diagram	9
Image Generator Test Block Diagram	10
Data rate setup	11
Number of lanes setup	11
Trigger setup for capturing 2 full frames	12
Two full frames captured without error	13
Capture Components setup: 100 bursts	14
Analysis of LP state transitions	15
Analysis of burst #26 showing an SOT marker followed by bytes (no errors in th	is burst)
	16
Analysis of burst #27 indicating errors were detected	17
CSI Packets View	17
The software is able to reconstruct a partial image despite the presence of error	rs18
Set up for color bar image transfer on 2 lanes at 800Mbps	19
Set up for color bar image properties	20
Setup for MIPI global timing parameters	21
	Auto SerDes links are used in ADAS systems to drive long cables (Source: MIPI Al FPD-Link III sub-system under test Block diagram FPD-Link III sub-system under test (DUT) Live Link Test Block Diagram Photo of Live Link showing probe insertion at input of SBC Image Capture Test Block Diagram Image Generator Test Block Diagram Data rate setup Number of lanes setup Trigger setup for capturing 2 full frames Two full frames captured without error Capture Components setup: 100 bursts Analysis of LP state transitions Analysis of burst #26 showing an SOT marker followed by bytes (no errors in th Analysis of burst #27 indicating errors were detected CSI Packets View The software is able to reconstruct a partial image despite the presence of error Set up for color bar image properties Setup for MIPI global timing parameters



Introduction

OVERVIEW

Over the last few years, growing concerns about automotive safety among consumers has resulted in high demand for advanced safety features, and as a direct result, car manufacturers and industry analysts are predicting an increase in demand of over 25% for ADAS-equipped automobiles by the year 2020.

Advanced driver assistance systems (ADAS) applications contribute to a safer environment for everyone sharing our roadways: drivers, passengers, and pedestrians alike. ADAS applications provide additional information about the surroundings of the car to the driver through surround view or rear-view systems and can warn the driver of dangerous situations through lane departure and blind spot warnings. This is accomplished by using an increasing number of data sources via sensors installed around the entire perimeter of the vehicle.

These data sources are typically connected to an Infotainment Telematics Hub via a Network Bridge which incorporates a MIPI to/from Auto SerDes translator. The Auto SerDes link provides power and control data to the sensors, but its main function is to drive high-speed data over the long length channels found in most automotive cable harness assemblies.

In this paper, we describe an Auto SerDes implementation based on an FPD link solution from Texas Instruments, and the concepts here are applicable to any Auto SerDes technology such as Apix-3 from Inova Semiconductor or SerDes solutions from Maxim Integrated to name a few.



Figure 1: Auto SerDes links are used in ADAS systems to drive long cables (Source: MIPI Alliance)



FPD-LINK

FPD-Link is the original high-speed digital video interface created in 1996 by National Semiconductor (now within Texas Instruments). It is a free and open standard for connecting the output from a graphics processing unit to the display panel's timing controller.

Automotive infotainment displays for navigation systems started using FPD-Link in 2001. BMW was the first car maker to use FPD-Link in their cars for transferring navigation graphics from the head unit to the central information display. Many other car manufacturers then started using FPD-Link. Today, most infotainment and driver assistance applications are using FPD-Link II and FPD-Link III to benefit from the embedded clock and control signals. One of the main benefits is the reduced cable size and weight due to the single wire pair for all the data and clock signals. (Source: https://en.wikipedia.org/wiki/FPD-Link)

ADAS SUB-SYSTEM

This document describes how Introspect DPHY test tools can be employed in testing such ADAS/FPD-Link systems. More specifically, we will be describing a commercial FPD-Link III sub-system, its interfaces, and how we can test them.

The FPD-Link III sub-system that we will be interfacing to is shown in the block diagram that follows.





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As shown in the Block diagram, the FPD-Link III interface is at the center of the sub-system, but the inputs and outputs of the sub-system are both MIPI-CSI interfaces. MIPI technology is a favorable component choice for car manufacturers as it allows them to leverage low-cost, high-performance image sensors and processors from the mobile phone industry.



To prove that the sub-system is fully operational, a MIPI CSI-2 stimulus is applied at the input of the subsystem and then the MIPI CSI-2 output from the sub-system is captured and analyzed (or processed by a MIPI receiving device).

This stimulus can come from multiple sources:

- Commercial Image Sensor (as shown in Figure 3)
- Introspect SV3C-DPTX MIPI DPHY Generator

The output can be captured and analyzed (or processed) using the following devices:

- Commercial MIPI CSI-2 Receiver
- Introspect SV3C-DPRX MIPI DPHY Analyzer

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Test Scenarios

This section describes various testing scenarios.

SCENARIO #1: LIVE LINK TEST

This test demonstrates how we can use the combination of Introspect PV1 Probes and a DPHY Analyzer to sniff the MIPI CSI-2 bus and perform packet data analysis without disrupting the live link. Several MIPI bus timing parameters are also extracted to validate conformance to specifications.



A block diagram of the Live Link Test hardware setup is shown below.

The Live Link Test hardware is composed of the following components:

- Image Sensor: Omnivision OV10640 installed on a daughter card and inserted into FPD-Link MIPI Input connector
- FPD-Link Tx: Texas Instruments DS90UB953EVM
- FPD-Link Rx: Texas Instruments DS90UB954EVM
- **iMX6 SBC:** A commercially available Single-Board Computer (SBC) containing a Freescale iMX6 application processor
- Probes: Introspect Technology PV1 Active Probe

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- **DPHY Analyzer:** Introspect Technology SV3C-DPRX
- Commercial Laptop: Any brand, running a Microsoft operating system

In this test, the sub-system is setup in normal operation, where a MIPI source transmits a stream of images through the FPD-Link sub-system. The sub-system MIPI output is sent to a commercial SBC where the received images are displayed on a commercial HDMI display.



Figure 5: Photo of Live Link showing probe insertion at input of SBC

In the photo for **Error! Reference source not found.**, a PCB is used to convert the MIPI CSI-2 Output from SMA cable to Ribbon cable as required for the SBC input. The probes are installed at this location. It is recommended to install the probes as close as possible to the MIPI Receiver input.



SCENARIO #2: IMAGE CAPTURE TEST

This test demonstrates how the Introspect DPHY Analyzer can be used as the endpoint which receives the sub-system MIPI output. The endpoint performs dynamic termination control as per MIPI specifications, and then captures image data from the sub-system based on flexible trigger mechanisms. Analysis is performed on every packet, showing errors where applicable. Received images are reconstructed for viewing.

 MIPI CSI-2
 FPD-Link
 MIPI CSI-2

 Image
 FPD-Link
 FPD-Link

 Tx
 FPD-Link
 DPHY

 Analyzer
 Image

 Figure 6: Image Capture Test Block Diagram

A block diagram of the hardware setup is shown below.

SCENARIO #3: IMAGE GENERATOR TEST

This test setup shows how the *Introspect DPHY Generator* can be used to stress the sub-system MIPI input. Stress sources can be voltage amplitude attenuation, clock to data skew, injection of controlled amounts of jitter, MIPI global timing parameter violations, invalid SOT marker, and so on. Functional tests can also be performed to test different image formats, frame rates, frame numbering, line rates, line numbering, blanking, encryption, and so on.

A block diagram of the hardware setup is shown below.

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In this block diagram, a new component is introduced which emulates the MIPI CSI Image Sensor.

• DPHY Generator: Introspect Technology SV3C-DPTX

Test Execution & Results

In this section, we describe software setup and test results from the different testing scenarios.

SCENARIOS #1 & 2: DPHY ANALYZER

Example1: Frame Capture

The Introspect DPHY Analyzer is set up to capture full frames as follows.

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THE LUIL TESP/IVITPI_DPHY_AN	IALYZER2 Wizards ControlPanels	fools Results He	lp Debug			
Params	Log	Results				
Components	globalClo	ockConfig properties (cla	ss: GlobalClockCon	fig)		
siDataCapture1	dataRate	800.	0			
obalClockConfig	uiWidth	1250	0.0			
ini Protocol	updateDataRateDependentDefaults	True				
	systemRefClockSource	intern	al			
	outputClockAFormat	LVDS				
	outputClockAFreq	100.0				
	outputClockBFormat	LVDS				
	outputClockBFreq	100.0				
	sscEnabled	False				
Add Remove Config	dataRate Sets the master operating data rate (Mbp min 48.82 Mbps, max 4166 Mbps	ps). All channels within t	he IESP operate at f	he same master d	lata rate. F	ange:
Add Remove Config	dataRate Sets the master operating data rate (Mbp min 48.82 Mbps, max 4166 Mbps	ps). All channels within t	he IESP operate at t	he same master d	lata rate. F	ange:
Add Remove Config est Procedure 1 globalClockConfig.se 2 csiDataCapture1.run	dataRate Sets the master operating data rate (Mbr min 48.82 Mbps, max 4166 Mbps	os). All channels within t	he IESP operate at t	he same master d	lata rate, F	ange:
Add Remove Config Test Procedure 1 globalClockConfig.se 2 csiDataCapture1.run 3	dataRate Sets the master operating data rate (Mbp min 48.82 Mbps, max 4166 Mbps etup () ()	os). All channels within t	he IESP operate at I	he same master d	lata rate. F	ange:

Figure 8: Data Rate Setup

	Log	Results	
Components	anel ist	1 properties (class: MiniDobyl anel ist)	
csiDataCapture1 globalCockCorfig Emetisti mipiProtocol	lanes is Data Split Across Lanes expected Pattern Ip Threshold Voltage hs Threshold Voltage continuous Clock	[1.2] True 600.0 50.0 False	
Add Remove Config Test Procedure 1 globalClockConfig.set 2 csiDataCapturel.run() 3	Ianes list of RX lane numbers (e.g. [1,2,3])		

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I didilis	Log	Result	ts	
Components	csiData	Capture1 properties (cl	ass: MipiDphyCsiDataCaptu	re)
csiDataCapture 1 globalCockCorfig laneList 1 mipiProtocol	laneList lanes expectedPattern captureMode triggerOndition preTriggerOuration postTriggerDype postTriggerDype postTriggerOuration csiRawFormatBayerCell timeout wantAnalysis imageFileFormat wantPixeIDataFiles pageFileFormat	L L L L L L L L L L L L L L L L L L L	aneList 1 [1, 2] purst trameStart le+04 3GGR 20 True PNG False True	-
Add Remove Config	post TriggerDuration This specifies the length of the post If "post TiggerType" is "durationInN "numberOfBytes", then this property "captureMode" is "burst".	trigger section. The uni s", then this property sh should specify the num	its for this are specified by th nould be specified in nanose nber of bytes, etc. This is onl	e "postTriggerType" property. conds. If "postTriggerType" is y relevant when
Test Procedure 1 globalClockConfig.set 2 csiDataCapturel.run() 3	up ()			
			-	

To run a test, the operator assigns component properties and then presses the Run button.

Analysis Results

When the capture runs without error, it is most interesting to look at the 'Frames' view, which presents a high-level summary of the captured image properties.

The following screenshot shows the reconstructed image. No errors were found in the 'HS Bursts', 'CSI Packets', 'LP States', and 'LP Events' analysis views.



	-	×
st mode: 1540 bursts, 1540 CSI packets, 4619 lpStates, 3079 lpEvents, 2 frames		
ane1 ane2 ane3 are4 Times: relative ToStart v Images: actual Size v		
kursts CSI Packets LP States LP Events Frames		
Time (ms) VC Index DT DT Name ImageWidth ImageHeight FirstPacket LastPacket		
0.000233 0 0 0x1E YUV422_8bit 1024 768 0 769		
33.337655 0 1 0x1E YUV422_8bt 1024 768 <u>770</u> <u>1539</u>		
Image size is correct		
Eramo rato is correct Data Type is correct		
me vcu_u_atux te		
		P.
		~
	_	
		>
		>

Frame View

In the above Frame Capture, the expected image size was 1024x768 and the expected image format was YUV422 (8bit). The Image Sensor was transmitting a color bar pattern at a frame rate of 30fps (period=33.33ms). There were no errors in the captured Bursts or Packets. This capture reveals that the link was functioning correctly.

Example2: Burst Capture

When errors are present in the Frame capture, or when a Frame capture is not possible, it is more useful to perform Burst captures. This example shows how burst captures can be used to debug a faulty system.

The following screenshots show how the *Introspect DPHY Analyzer* is set up to capture bursts of data. A burst is defined as a transition out of the low power



Introspect ESP (v 3.5.85) - sv3-dprxAdasCaptures (SV3C 4L3G MIPI DPHY ANALYZER2) × File Edit IESP/MIPI_DPHY_ANALYZER2 Wizards ControlPanels Tools Results Help Debug Params Log Results Components csiDataCapture1 properties (class: MipiDphyCsiDataCapture) csiDataCapture1 laneList laneList1 globalClockConfig lanes [1, 2] lanel ist 1 nipi Protocol expectedPattern captureMode burst triggerCondition anyBurst preTriggerDuration 1e+04 postTriggerType numberOfFrameEnds postTria 100 csiRawFormatBayerCell BGGR timeout 20 wantAnalysis True imageFileFormat PNG want Pixel Data Files False saveResults True post TriggerDuration This specifies the length of the post-trigger section. The units for this are specified by the "post Trigger Type" property. If "post Trigger Type" is "durationInNs", then this property should be specified in nanoseconds. If "post Trigger Type" is "numberOfBytes", then this property should specify the number of bytes, etc. This is only relevant when "captureMode" is "burst". Add Remove Config Test Procedure 1 globalClockConfig.setup() 2 csiDataCapture1.run() 3 MIPI DPHY Csi2_v2_0 Run 0

Stop state and into the High-Speed Data Transfer state and then back to the low power Stop state.

Figure 12: Two full frames captured without error

Analysis Results

The first result below shows a burst mode capture of 100 bursts. The report shows that there were errors in some of the bursts/packets. Despite the presence of errors, the software attempts to reconstruct the received image based on valid data received.

To debug this scenario, we can leverage the selection of views provided by the analysis software.

First, we look at the 'LP States' view. Here we see valid transitions from the Stop state (LP11) to HS-Request state (LP01) to HS-Prepare state (LP00). From the time column, we can see the global timing parameter TLPX = 60ns (time spent in LP01 state), which is within specifications. We can also observe that the sequence (LP11-LP01-LP00) timing is repetitive, which is expected behavior during a frame



transmission as this is the line timing. From the line timing, one can separate active pixel time (LP00) from blanking time (LP11).

We conclude that the problem is not LP related.

burst	mode: 100 bu	rsts (12	errors), 88 CSI p	ackets (34 erro	s), 299 lpStates, 1	199 lpEvents, 1 fr	ame							
Iar	ne1 🔘 lane	2 ()	lane3 🔘 lane	-4	Go To: Timesta	amp V	Times:	: relative	FoStart ∨					
HS Bu	sts CSI Pac	ket s L	P States P E	vents Frames										
ID	Time (ms)	BitsP	N Duration (ns) LP Event										
0	0.000000	00	5145	<u>0</u>										
1	0.005145	11	24015					\backslash						
2	0.029160	01	60	1									1	
3	0.029220	00	5145	2				E	rors we	ere dete	ected in	some		
4	0.034365	[11]	23895											
5	0.058260	01	60	3										
6	0.058320	00	5145	4										
7	0.063465	(11)	24015											
8	0.087480	01	60	<u>5</u>										
9	0.087540	00	5145	<u>6</u>										
10	0.092685	11	23895											
11	0.116580	01	60	Z	<u> </u>									
12	0.116640	00	5145	<u>8</u>		Valid LP	transiti	ions f	or HS d	lata				
13	0.121785	11	23955											
14	0.145740	01	60	9										
15	0.145800	00	5145	<u>10</u>										
16	0.150945	11	24015											
17	0.174960	01	60	11		TIPX =	60ns							
18	0.175020	00	5145	<u>12</u>										
19	0.180165	11	23895											
20	0.204060	01	60	<u>13</u>										
21	0.204120	00	5145	14										

Figure 13: Analysis of LP state transitions

Next, we look at the HS activity by selecting 'HS Bursts' view. This view shows some red cells (bursts with errors) and some normal cells. We will look at both cases below.

Burst With No Errors

Burst #26 shows a normal capture where all PHY-level events are without error. An SOT marker was detected, and the number of bytes that follow are counted and stored for further analysis.





Burst With Errors

In burst #27, no SOT marker was found during the analysis (clicking on the SOT button yields no results), therefore NumBytes and SotOffset cannot be determined. This burst can not be used to form a CSI packet, and therefore we expect some lines will be missing in the reconstructed image. All bits captured on this lane can be viewed in the "bits" field in the lower window. You can use the "Find..." button to search for any bit combination in the bitstream.



HS Bursts	CSI Packets	LP States	I P Events	Frames							
Burst ID	Time (ms)	NumBytes	NumBits	SotOffset	NumCsiPackets						-
23	0.670735	492	4136	187	1						
24	0.699835	492	4136	187	1						
25	0.728995	492	4136	187	1						
26	0.758215	492	4136	187	1						
27	0.787315		4136		0						
28	0.816535	492	4136	187	1						
29	0.845635	492	4136	188	1						
30	0.874795	492	4136	188	1						
31	0.904015		4136		0						
32	0.933115	493	4144	188	1		No SOT Marke	r was detected	l in this		
33	0.962335	493	4136	181	1						
34	0.991435	492	4128	181	1		1				
35	1.020595	493	4136	181	1		/				
36	1.049815	492	4128	181	1						
37	1.078915	493	4136	181	1						
38	1.108135		4128		0						
Burst 27 [Diffset: 187 byte byte byte	0etail (4136) bits:00 index: (hex): (dec):	<< 00011000	 0011010	0011111	11111111	111111111	>>/ SOT Fi	nd 1111111111111111111111111111111111	1111 <u>1111111</u> 111	111111	.11

Packet View

Next, we move up a level to the 'CSI Packets' view. This view also shows some errors (red cells).

burst mode: 10	0 bursts (12 e	rrors), 8	8 CSI pa	ckets (34 errors), 2	99 lpStates, 1	99 lpEvents,	1 frame							
● lane1 ○	lane2 🔘 la	ine3 () lane4		Go	To: Next Err	or	∼ Tin	es: relative1	ToStart ∨					
HS Bursts CS	Packets LF	States	LP Ev	ents	Frames										
Packet ID	Time (ms)	Burst	VC	DT	DT name	Header EC	c wc	Payload CR	C Short						
0	0.000239	0	0	0x2C	RAW12	0x0D	1920	0xB866							
1	0.029459	1	0	0x2C	RAW12	0x0D	1920	0xC390							
2	0.058559	2	0	0x2C	RAW12	0x0D	1920	0xB866							
3	0.087779	3	0	0x2C	RAW12	0x0D	1920	0xC390							
4	0.116879	4	0	0x2C	RAW12	0x0D	1920	0x8844							
5	0.146039	5	0	0x2C	RAW12	0x0D	1920	0xC390							
6	0.175260	6	0	0x2C	RAW12	0x0D	1920	0x8866							
7	0.204360	Z	0	0x2C	RAW12	0x0D	1920	0xC390							
8	0.233581	8	0	0x2C	RAW12	0x0D	1920	0xB866							
9	0.262680	9	0	0x2C	RAW12	0x0D	1920	0xC380							
10	0.291840	10	0	0x2C	RAW12	0x0D	1920	0x8866							
11	0.321060	11	0	0x2C	RAW12	0x0D	1920	0xC300							
12	0.350161	12	0	0x2C	RAW12	0x0D	1920	0xB866							
12	0.270201	12	0	0-3C	PAW12	0-00	1920	0-0200							
Data n															
Offset V		<	~~~~		<	2	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	22		-			10		10
	0	1		2		3	4	5	6	/	8	9	10	11	12
iane1 dal	a: 34	_	22	-	22	22	2.2	22	22	22	22	22	22	22	
iane2 dat	a: 01	_		-											
lane3 dal	a: E0	_	22	-	22	22	2.2	22	22	22	22		22	22	
iane4 dat	a: 80	00 5				TTTTTTTT		TT TT		PEFFFFFF	TETTETT	FFFFFFFF		E E	
Dyte	s: 208007	00 2		2 22											

Figure 16: CSI Packets View



CSI Packets are constructed by merging valid HS Burst data from all lanes. The packet header is analyzed and key parameters such as Virtual Channel (VC), Data Type (DT), and Word Count (WC) are extracted and presented. When the ECC field in the packet header or the CRC field in the packet payload does not match with the value computed by the Analyzer, an error is flagged (highlighted in red).

Frame View

Finally, we can move up one more level to the 'Frames' view. Frames are constructed by merging valid CSI Packets, usually delimited by 'Frame Start' and 'Frame End' packets.

DPH	IY DataCapt	ture: R	un_201	7-09-1	1_1431_52	errorsLane	1 / csiDataCapt	ure1							-	
urst mo lane Burst	ode: 100 bun 1 Olane2 s CSI Pack	sts (12 2) cets L	errors), i lane3 .P State	88 CSI Iar s LP	packets (3 ne4 Events F	4 errors), 299 rames	lpStates, 199 lpE	vents, 1 frame	Times: rela	tiveToStart	~	Images: f	tToWindow	~		
D	Time (ms)	VC	Index	DT	DT Name	Image Widt	n ImageHeight	FirstPacket	LastPacket							
	0.000239	0	D	0x2C	RAW12	1280	54	<u>0</u>	<u>87</u>							
rame v	vc0_0_dt0x2	с														

Figure 17: The software is able to reconstruct a partial image despite the presence of errors.

In the Frames view, we see the reconstructed image. We can observe an image width of 1280 pixels (which is correct) and a height of 54 lines (partial image). The image is partial because we limited the capture to 100 bursts and some bursts/packets had errors. Despite the errors, we can see that the image is what we are expecting (i.e. a color bar image), which is encouraging.

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Later in the debugging process, it was found that an intermittent connection was the source of the CRC errors in the packet view and the missing lines in the frame view. The SV3C-DPRX was indispensable in rapidly pinpointing the source of the issue and ruling out any protocol or global timing errors.

SCENARIO #3: DPHY GENERATOR

The following screenshots show how the Introspect DPHY Generator can be set up to emulate the same Image Sensor.

File Edit IESP/MIPI_DPHY_GENE	RATOR Wizards ControlPanels Tools	Results Help Debug		
Params	Log	Results		
Components	mipiDphyGenerato	or1 properties (class: MipiDphyGenerator)		
components dphyCstColorBarPattern 1 dphyParameters 1 titternjection 1 mipiDphyGenerator 1 mipiPphyGenerator 1 mipiPptocool	mipupnySeneration dataLanes dataBate splitDataAcrossLanes continuousClock dphyPattem resetPattemMemory dphyParams hsDataVoltageAmplitudes hsDataVoltageAmplitudes hsClockVoltages hsClockVoltages hsClockVoltages hsClockVoltage hsClockVoltage hsClockVoltage hsClockVoltage hsClockVoltage hsClockVoltage hsDataPostTaps hsClockPostTap hsClockPostTap dataSkews clockSkew	Important Class: MippingGenerator) 800.0 - - True False dphyCsiColorBarPattern 1 True dphyParameters 1 - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [200.0] - - [0.0] - - [0] - - [0] - - [0] - - [0] - - [0] - - [0] - - [0] - -		
Add Remove Config Test Procedure 1 mipiDphyGenerator1.se 2	dataRate Sets the MIPI data rate (Mbps). Range: min 80.1 cup ()	0 Mbps, max 6500.0 Mbps		

Figure 18: Set up for color bar image transfer on 2 lanes at 800Mbps

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	Log	Results		
Components	dphyCsiColorBarPattem	1 properties (class: MipiDphyCsiColo	rBarPattem)	
dphyCsiColorBarPattern1	image Height	768		
dphyParameters1	imageWidth	1024		
jitterInjection1	timeUnits	nanosecond		
mipiDphyGeneratori	imageFormat	CSI YUV422 8bit		\sim
	usePreBuiltColorBar	True		
	preBuiltColorBar	ColorBar_ctsHsTestPatte	em	
	lineTimeMode	lineTime_constant		
	horizLineTime	30000.0		
	frameBlankingMode	frameRate		
	frameRate	30.0		
	lineNumbering	disabled		
	wantFrameNumbering	False		
	useEpdInsideLines	False		
	useEpdBetweenLines	False		
	useEpdBetweenFrames virtualChannel	False 0		
	useEpdBetweenFrames virtualChannel	False 0		
Add Remove Config	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		
Add Remove Config Test Procedure	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		
Add Remove Config Test Procedure 1 mipiDphyGenerator1.set 2	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		
Add Remove Config Test Procedure 1 mipiDphyGenerator1.set 2	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		
Add Remove Config Test Procedure 1 mipiDphyGenerator1.set 2	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType) :up ()	False 0		
Add Remove Config Test Procedure 1 mipiDphyGenerator1.set 2	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		
Add Remove Config	useEpdBetweenFrames virtualChannel imageFormat Image format (determines the dataType)	False 0		

Figure 19: Set up for color bar image properties



Params	Log	Results	
Components	dobyParam	eters1 properties (class: MiniDohyParameters)	
dphyCsiColorBarPattern1			
dphyParameters1	sotBits	00011101	
jitterInjection1	tlpxDuration	60.0	
mipiDphyGenerator1	tHsLpx01Duration	(0.0, 60.0)	
mipiProtocol	tHsPrepareDuration	(5.0, 60.0)	
	tHsZeroDuration	(10.0, 145.0)	
	tHs IrailDuration	(8.0, 60.0)	
	tHsidlePostDuration	8	
	thsidieCikHsuDuration	(0.0, 60.0)	
	tCleaks are 10 provided	ŏ (0.0. 90.0)	
	tClockLpxuTDuration	(0.0, 80.0)	
	tClock Frepare Duration	(0.0, 80.0)	
	tClock TrailDuration	(0.0, 300.0)	
	tClock PreDuration	(32.0.00)	
	tClockPostDuration	(60.0, 60.0)	
	tHsExitDuration	240.0	
	tTaGoDuration	40	
	t Ta Sure Duration	1.0	
	tTaGetDuration	5	
	hsZeroBits	0000	
	hsTrailBits		
	clockZeroBits	0000	
	clock Trail Bits		
Add Remove Conf	tHsLpx01Duration Tuple (a,b) where (a*UI + b ns) specifies th g	ne duration of the HS burst LP01 state on the data lar	ies
Test Procedure 1 mipiDphyGenerator1 2	setup()		
-	_		

The process is quite simple, after all properties are setup, the operator presses the 'Run' button and the image is transferred continuously.



Default values are always valid and within specifications. These can be used for testing with nominal conditions. The values can be changed to best-case, worst-case, or even out-of-spec values for stress testing any MIPI CSI-2 Receiver.

For higher data rates, a jitter injection component and calibration burst can be enabled as well.

Conclusion

This paper described an Automotive SerDes link and how it interfaces to electronic processing components using MIPI conduits. We also showed an end-to-end testing scheme for such SerDes link, deploying Introspect generators and analyzers to respectively stress receiver electrical parameters and analyze transmitter protocol and physical layer behavior. We illustrated the use of active probes to monitor live traffic, and we also demonstrated the use of Introspect analyzers as terminating endpoints, featuring fully integrated switchable termination resistors as per the MIPI Alliance specifications.

For more information about development, verification, and production instruments and equipment for SerDes and MIPI applications, visit the Introspect Technology website, www.introspect.ca, and our resources page at www.introspect.ca/resource-center

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